
*12th International Symposium on*

# Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC 2017)

*July 12-14, 2017, Madrid, Spain*

## Technical Program

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## Wednesday, July 12th 2017

***8:45 Registration***

***9:15 - 9:30*** **Opening**

***9:30 – 10:30*** **Keynote talk –** *Extending Operating System Services over FPGAs.* Marco Platzner. Paderborn University. **(Chair: Eduardo de la Torre)**

***10:30 – 11:00 Coffee break***

**11:00 – 12: 30 Session 1: Reconfigurable On-Chip Communication Architectures (Chair: Leandro Indrusiak)**

> **Exploring the Performance of Partially Reconfigurable Point-to-Point Interconnects.** *El Mehdi Abdali, François Berry, Maxime Pelcat, Jean-Philippe Diguet and Francesca Palumbo.*
>
> **Fault-resilient NoC router with transparent resource allocation**. *Tsotne Putkaradze, Siavoosh Payandeh Azad, Behrad Niazmand, Jaan Raik and Gert Jervan.*
>
> **Adaptive and Reconfigurable Bubble Routing Technique for 2D Torus Interconnection Networks**. *Poona Bahrebar and Dirk Stroobandt.*

***12:30 – 14:00 Lunch***

***14:00 - 15:00*** **Keynote talk –** *"The rebirth of hardware: Open-source hardware initiatives for IoT- and MINT-based developments"*. Manfred Glesner. Technische Universität Darmstadt. **(Chair: Marco Platzner)**

**15:00 – 16:00 Session 2: Applications (Chair: Marco Platzner)**

> **Current Mode Detection in Hard Real-time Automotive Applications Dedicated to Many-Core Platforms.** *Piotr Dziurzanski.*

**Programmable SoC platform for Deep Packet Inspection using enhanced Boyer-Moore algorithm.** *Adrian Dominguez, Pedro P. Carballo and Antonio Núñez.*

***16:00 – 16:30 Coffee break***

**16:30 – 18:00 Session 3: Multi-core and Many-core Systems (Chair: Thilo Piontek)**

**ElasticSimMATE: a Fast and Accurate gem5 Trace-Driven Simulator for Multicore Systems.** *Alejandro Nocua, Florent Bruguier, Abdoulaye Gamatié and Gilles Sassatelli.*

**High-Level Test Generation for Processing Elements in Many-Core Systems.** *Adeboye Stephen Oyeniran, Raimund Ubar, Siavoosh Payandeh Azad and Jaan Raik.*

**Characterization and Optimization of Behavioral Hardware Accelerators in Heterogeneous MPSoC.** *Yidi Liu, Monica Villaverde San Jose, Felix Moreno and Benjamin Carrion Schafer.*

***19:00 – 21:00* Welcome Cocktail**

## Thursday, July 13th 2017

***9:30 – 10:30*** **Keynote talk** - *Space, the final frontier, the best testbed: Applications, Challenges and Needs for the application of reconfigurable SoCs to Space.* Ángel Álvaro. Thales Alenia Space **(Chair: Eduardo de la Torre)**

***10:30 – 10:50 Coffee break***

***10:50 - 11:00*** *"ReCoSoC in one year from now: insight on the 2018 edition"*

***11:00 – 12:30*** **Special Session 1: High Level Design Methodologies for Reconfigurable Computing and Adaptive Systems: tool flows and applications (Chair: Kurt Ackermann)**

**System-Level Design for Communication-Centric Task Farm Applications.** *Daniela Genius and Ludovic Apvrille.*

**Analysis of heterogeneous multi-core multi-HW accelerator based systems designed using PREESM and SDSoC.** *Leonardo Suriano, Alfonso Rodriguez, Karol Desnos, Maxime Pelcat and Eduardo de La Torre.*

**High-Level Design using Intel FPGA OpenCL: a Hyperspectral Imaging Spatial-Spectral Classifier.** *Rubén Domingo, Rubén Salvador, Daniel Madroñal, Raquel Lazcano, Eduardo Juárez, Cesar Sanz, Himar Fabelo, Samuel Ortega and Gustavo M. Callicó.*

***12:30 – 14:00 Lunch***

***14:00 -15:00*** **Keynote talk –** *Networks-on-Chip for Real-Time and Mixed-Criticality Applications.* Leandro Indrusiak. University of York. **(Chair: Gilles SASSATELLI)**

***15:00 – 16:30*** **Session 4: Reconfigurable and Self-Aware Systems-on-Chip (Chair: Eduardo Juarez)**

**Design and Scalability Analysis of Bandwidth-Compressed Stream Computing with Multiple FPGAs.** *Antoniette Mondigo, Tomohiro Ueno, Daichi Tanaka, Kentaro Sano and Satoru Yamamoto.*

**On-Demand Instantiation of Co-Processors on Dynamically Reconfigurable FPGAs.** *Marcel Essig and Kurt Ackermann.*

**Computational Self-Awareness as Design Approach for Visual Sensor Nodes**. *Zakarya Guettatfi, Philipp Hübner, Marco Platzner and Bernhard Rinner.*

***16:30 – 17:00 Coffee break***

***17:00 – 18:00*** **Session 5: Emerging Technologies (Chair: Gilles SASSATELLI)**

**Design Method for Asymmetric 3D Interconnect Architectures with High-Level Models.** *Jan Moritz Joseph, Lennart Bamberg, Sven Wrieden, Dominik Ermel, Alberto Garcia-Oritz and Thilo Pionteck.*

**Energy Aware and Reliable STT-RAM based Cache Design for 3D Embedded Chip-Multiprocessors.** *Fatemeh Arezoomand, Arghavan Asad, Mahdi Fazeli, Mahmood Fathy and Farah Mohammadi.*

***19:00 Social Event and Gala Dinner***

## Friday, July 14th 2017

***9:00 – 10:00*** **Keynote talk –** *Safety, security and availability – How will this fly for autonomous cars?* Albrecht Mayer. Infineon Technologies **(Chair: Martha Johanna Sepulveda)**

**10:00 – 11:00 Special Session 2: Fault and Security Management in NoCs and MPSoCs (Chair: Martha Johanna Sepulveda)**

**Towards Trace-driven Cache Attacks by Exploiting Bus Communication on Systems-on-Chips.** *Johanna Sepulveda, Mathieu Gross, Andreas Zankl and Georg Sigl.*

**Fault Recovery and Adaptation in Time-Triggered Networks-on-Chips for Mixed-Criticality Systems.** *Hamidreza Ahmadian, Farzad Nekouei and Roman Obermaisser.*

***11:00 – 11:30 Coffee break***

***11:30 – 13:00*** **Session 6: More Secure SoCs and NoCs (Chair: Gert Jervan)**

**Federated system-to-service authentication and authorization combining PUFs and tokens.** *Marta Beltran, Miguel Calvo and Sergio González.*

**Side-Channel Attack Resilience through Route Randomisation in Secure Real-Time Networks-on-Chip.** *Leandro Indrusiak, James Harbin and Martha Johanna Sepulveda.*

**SecBoot - Lightweight secure boot mechanism for Linux-based embedded systems on FPGA.** *Peter Rouget, Benoît Badrignans, Pascal Benoit and Lionel Torres.*

***13:00 – 13:15*** **Closing Session**

***13:15 – 14:45 Lunch***