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Supercomputing and European Sovereignty

Mateo Valero

Abstract

Over that last 3 decades, we have witnessed a transition from closed software ecosystems being the foundation for HPC, enterprise, and business to open source software ecosystems based on Linux: from Arduino in the IoT space, to Android in the mobile space to Linux in HPC and cloud-based systems with various Open Source Software projects built on top. However, when examining hardware, current commercial off the shelf solutions are closed hardware ecosystems that only enable integration at the peripheral (PCIe) level. The combination of current technology trends, the slowing of Moore's Law, and cost prohibitive silicon manufacturing inhibit significant power-performance gains by relying on traditional closed ecosystems, especially in HPC, technology pushed to the extreme. This new regime forces systems to be much more specialized to achieve the power-performance profiles required for a supercomputer. In the past, HPC has led the way forward, defining the bleeding edge of technology. HPC can do this again with open hardware, as it has done in software with adopting Linux and open source in general. This is not only a technology imperative, but one born out of current geopolitics. Digital Technology (the generation and processing of data) is the basis for global commerce, scientific discovery, and ubiquitous in modern life. Thus, creation of digital technology in the form of processors, accelerators and the related digital infrastructure guarantees access to these building blocks of the digital economy regardless of the geopolitical environment. Given this technology and geopolitical backdrop, we describe how Europe can exploit its resources targeting research and development for technological independence.

In this today's technology environment, some of the rules have changed. This has produced a shift from abundant transistors to efficient use of transistors. Thus, to truly meet the power and performance requirements, we must specialize the hardware. At the same time, the software stack is evolving, becoming more abstract, enabling higher programmer productivity, but sacrificing hardware efficiency. Thus, application owners will need to co-design the full stack, all layers of hardware and software, in order to meet their performance and power (e.g., FLOPs/W) targets. This level of integration is not possible in a closed or even partially open ecosystem. The platform must be open to enable this tight integration. We see this openness today in the Linux OS, toolchain, runtimes, frameworks, and libraries, up to the application layer. This enables rapid development and extension of software systems. However, an open hardware infrastructure was lacking, making specialization nearly impossible, especially in a research context. Openness is required to tailor your hardware platform to the applications, thereby achieving the desired performance in the power constrained environment. There have been a couple of open source hardware platforms in the past, but Moore's Law inhibited their adoption for many reasons: general purpose processor improvements, time to market, cost, software development, etc. Furthermore, unlike Linux, previous open source hardware was entangled in the companies that created them. Mirroring the same model as Linux, RISC-V has followed a similar development path and has enjoyed significant industrial and academic adoption. Like Linux before it, the RISC-V ecosystem is in the nascent period where it can become the de facto open hardware platform of the future. The RISC-V ecosystem has the same opportunity in hardware that Linux created as a foundation for open source software. This enables the co-design of the RISC-V hardware and the entire software stack, creating a better overall solution than the closed hardware approach that is done today. RISC-V enables everyone to build what they want and need vs. buy something that partially meets their requirements. As European HPC recognized in the past with Linux, Europe has the opportunity to lead the charge, creating a full stack solution for everything from supercomputers to IoT devices, all based on an open ISA, providing interoperability and a freedom to create, build, and deploy superior technology based on European IP.

In this talk, first, we will provide background on HPC computing and the research we have conducted to shape the current state of the art in HPC. Using RISC-V as an instrument, we provide a vision for the future

and a collection of current research and innovation projects, infrastructure, and the community that are building the foundation for the future. This is a new opportunity for Europe to lead the way to an HPC Future that is Wide Open!

Mateo Valero, http://www.bsc.es/cv-mateo/. Director of the Barcelona Supercomputing Center. His research focuses on high performance architectures. He has published approximately 700 papers, has served in the organization of more than 300 International Conferences and he has given more than 600 invited talks. Prof. Valero has been honored with several awards, among them the 3 most relevant awards in Computer Architecture field: The Eckert-Mauchly Award 2007 by the IEEE and ACM, the Seymour Cray Award 2015 by IEEE and the Charles Babbage 2017 by IEEE. Among others: The Harry Goode Award 2009 by IEEE, The Distinguish Service Award by ACM and the Spanish National awards "Julio Rey Pastor" and "Leonardo Torres Quevedo". "Hall of the Fame" member of the ICT European Program (selected as one of the 25 most influents European researchers in IT during the period 1983-2008, Lyon, November 2008). In 2020 he has been awarded for his exceptional leadership in HPC by "HPCWire Reader's Choice Awards" for "being an HPC pioneer since 1990 and the driving force behind the renaissance of European HPC independence". Honored with "Condecoración de la Orden Mexicana del Águila Azteca" 2018, highest recognition granted by the Mexican Government. He is Honorary Doctorate by 10 Universities. He is member of 9 academies. He is a fellow of IEEE and ACM, and Fellow of AAIA, Asia-Pacific Artificial Intelligence Association.

In 1998 he won a "Favourite Son" Award of his home town, Alfamén (Zaragoza) and in 2006, his native town of Alfamén named their Public College after him.

RISC-V and Open hardware: The path for cooperative research, training and innovation around Open-source Hw/Sw

Lluís Terés

Abstract

The RISC-V ISA was born on 2010 at UC Berkeley aiming not just to create a new RISC machine, but an open, advanced, refined and modular instruction set to definitively address the open hardware challenges from the point of view of processor development. In 2016 the RISC-V Foundation came up to guide the open ISA standard independent evolution. Right now, thousands of members worldwide from industry and academia are part of the RISC-V Foundation ecosystem. Since then, many hardware implementations of RISC-V ISA have been made available as open source code ready for its physical materialization either in FPGA or in SoC, as well as components at chip level ready for systems development.

It seems clear that open-ISA RISC-V is an excellent opportunity to address open-source hardware to emulate the successful effect of Linux into software open-source as:

- It will democratize processor development by reducing cost entry barriers to mitigate the third party or country dependencies facilitating and opening market competition; thus, reducing the current oligopoly of a few companies/countries.
- It is a big opportunity for the research community to work together and develop such an open-hardware ecosystem and infrastructure to address not only RISC-V or processor-based developments, but also any SoC or hardware target design.
- The EU Chips Act is betting on open architectures such as RISC-V for its future processors, especially since UK and ARM are no longer part of the European Union and more recently due to semiconductors shortage and related technological sovereignty, currently seriously compromised.
- It is a great challenge to advance in open hardware in other fields beyond the processors, but taking advantage of the RISC-V push. RISC-V acts as a tractor for open hardware, but the concept of open-HW must go further and address any other HW domain.

Now, we have the chance to get involved from the early stages into this new wave of open hardware around RISC-V and beyond it by addressing simultaneously and collaboratively the basic pillars of Training, Research and Innovation working together from academy, research and industry. Red-RISCV was born, based on the above pillars, to stimulate the dissemination, training, philosophy and collaborative activities around the RISC-V initiative in particular and Open-hardware in general.

Dr. Lluís Terés Terés received an MS degree in 1982 and the PhD in 1986, both in Computer Sciences, from the Autonomous University of Barcelona (UAB). He is working in UAB since 1982 and in IMB-CNM (CSIC) since its creation in 1985. He is Head of Integrated Circuits & Systems (ICAS) group at IMB with research activity in the fields of ASIC's, sensor signal interfaces, body-implantable monitoring systems, integrated N/MEMS interfaces, flexible platform-based systems & SoC, organic/printed microelectronics and RISC-V cores development. He has participated in more than seventy industrial and research projects. He is co-author of more than eighty papers and eight patents. He has participated in two spin-offs. He is also an Associate Professor at the Univ. Autònoma de Barcelona (UAB) and coordinator of the Spanish research network Red-RISCV.

Open Hardware and Space: RISC-V, Airbus Crisa view

Juan Antonio Ortega

Abstract

During the last 20 years space applications have been based on radiation hardened hardware. Space is a harsh environment, extreme temperature ranges, high radiation levels, protons, neutrons, cosmic rays, and the vacuum of the space itself, place the on-board electronics into extreme conditions. On-board electronics must be able to work in that environment, and to work in a reliable way, maximizing availability during the whole satellite mission span, usually in the range of years.

Rad hard components are special, rare, expensive, and not such performant as the state of the art hardware used in nowadays commercial applications, in addition, the development cycles take too long, and current EDA tools do not support them all.

The traditional rad-hard hardware has been sufficient to develop the space applications that the market has been demanding until now. However the space market is changing and demands new systems and with short development cycles. Satellite constellations, new communication systems, new security systems, new imaging sensors, new autonomous systems, all of them demand for a complete new set of solutions, based on fast computing, machine learning, processing on source, in summary, a different computing paradigm.

Open hardware movement has tried to revolutionize the HW development in the way FSF and Open Source SW did. Open Hardware allows to build on reuse, is adopted by industry and institutions, is used for education, creating a big pool of students and engineers, and a big support community, in opposition to proprietary solutions. Open ISA standard Sparc has been the base of the computing in the European space industry during the last 20 years. Now other open ISA, RISC-V, has emerged and is increasing momentum at a very high speed. Because of its modularity, the existence of open source development tools, the support of a big part of industry, institutions, space agencies, and a big supporting community, it is in a very good position to become the new computing paradigm for European space applications.

RISC-V, due to its modularity, might help extend the operational life of traditional rad hard HW, and together with COTS, can bring the computational power demanded by future space applications