V²Iₚ Control: A Novel Control Technique with Very Fast Response under Load and Voltage Step

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Introduction

Starting point

Integrated DC/DC converter

Aim

Component size reduction

Integrated DC/DC converter + Output capacitor
Bandwidth requirements

**Voltage mode control**

- Maximum BW limited by parasitics
- Typical BW up to 300kHz

**Diagram**

- Parasitic ESL
  - $F_{res} = 1.8$ MHz
- Maximum BW limited by parasitics
  - $F_{s}=5$ MHz
  - Typical BW up to 300kHz

**Graph**

- Vp(VOUT) vs Frequency
  - 1MHz
  - 100kHz
  - 30kHz
  - 10kHz
  - 3kHz

**IV Annual Meeting**
- 2011 March
Contents

- Fast transient response techniques
- V2Ic Control
- Design Examples:
  - 5 MHz sync buck converter
- Experimental results
- Conclusions
Fast transient response techniques: $V^2$

Non-linear control techniques: $V^2$ control

- **Advantages**
  - Fast dynamic response
  - Simplicity

- **Disadvantages**
  - Triangular output voltage ripple is needed (ESR dominant)

Instability due to non-dominant ESR

PWM

V$^2$ control

Load

Reference

PWM

$V_{OUT}$

$V_{OUT}$

$V_{REF}$

$V_{OUT}$

Control

$R(s)$
Fast transient response techniques

2. Linear and non-linear: Hysteretic $I_C$

Fast transient response techniques

2. Linear and non-linear: Hysteretic $I_C$

- Advantages
  - Fast dynamic response

- Disadvantages
  - Variable switching frequency
  - High sensitivity to parasitic effects
Non-invasive output capacitor current sensor

Fast transient response techniques: VIc

ECCE’10 Fast control technique based on peak current mode control of the output capacitor current del Viejo, M.; Alou, P.; Oliver, J.A.; Garcia, O.; Cobos, J.A.;

Compensating slope is needed to avoid sub-harmonic oscillation over 50% duty cycles.

- Helps to desensitize to current sensor mismatches and parasitic effects.
- The higher the compensating slope, the worse the dynamic response.

Trade-off

It is necessary a compromise!
The evolution from VIc to V2Ic

**VIc Control**

**V2Ic Control**
V2IC operation: load step

V^2 IC Control

Fast reaction 200ns/div

Load Step
V2Ic operation: reference step

**V^2I_C Control**

**Fast reaction**

200ns/div
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5MHz Design example

$V_{in} = 3V$
$V_{out} = 1V,$
$f_{sw} = 5MHz,$
$L = 100nH$
$C_{out} = 4\mu F.$
Compensating ramp 600mV
$K_{Verror} = 1$
current loop gain ($K_{sensor}$) is 0.2V/A.
5MHz Design example: Output Impedance

V^2Ic Control

Equivalent to 1.5MHz BW

Open Loop Output Impedance

b) Fast loop closed and slow loop open

Zout

30dB

12dB
Comparison at 5MHz: VMC, V1c and V21c

Comparison of the proposed techniques with 1MHz bandwidth voltage mode control

Output voltage response under load step (4A)

Output voltage response under voltage reference step (1V)

Specifications:
- \( f_{\text{sw}} = 5\text{MHz} \)
- \( V_{\text{in}} = 3\text{V} \)
- \( V_{\text{out}} = 1\text{V} \)
- \( C_{\text{out}} = 4\mu\text{F} \)
- \( L = 100\text{nH} \)
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V2Ic 1MHz Design: Experimental Results

Specifications:
- $f_{sw} = 1\text{MHz}$
- $V_{in} = 3\text{V}$
- $V_{out} = 1\text{V}$
- $C_{out} = 4\mu\text{F}$
- $L = 440\text{nH}$

Voltage reference step

![Diagram showing voltage reference step and waveform characteristics.](image-url)
Conclusions

V\textsuperscript{2}Ic Control

- **Advantages**
  - Integrated DC/DC converter
  - Fast dynamic response (feedforward of the load current)
  - Constant switching frequency
  - Low sensitivity to parasitics (compensating slope
  - Non-invasive output capacitor current sensor
  - Fast ref tracking

- **Cout reduction**

![Diagram of V\textsuperscript{2}Ic Control](image)
1MHz Design: Comparison V2Ic vs V2

Oscillation due to non dominant ESR (100mV/div)

V^2 I_c control
ΔB=10kHz

V^2 control
ΔB=10kHz

load step of 4A (40A/μs)

10μs/div

(100mV/div)
Oscillation due to non dominant

$V^2 I_c$ control
$\Delta B = 10 \text{kHz}$

$V^2 I_c$ control
$\Delta B = 10 \text{kHz}$

ref step 1V (2.5V/μs).
**V2Ic 1MHz Design: Experimental Results**

Specifications:
- $f_{sw} = 1\text{MHz}$
- $V_{in} = 3\text{V}$
- $V_{out} = 1\text{V}$
- $C_{out} = 4\mu\text{F}$
- $L = 440\text{nH}$

Positive load step of 1A and 40A/µs

Negative load step of 1A and 40A/µs
5MHz Design example: Load Step response

V^2I_C Control

Load step

di/dt=40A/µs (2µs/div)

180mV

3µs

4A
VIc vs high bandwidth voltage mode control

$\text{VI}_c \rightarrow \Delta B = 50k\text{Hz}$

$\text{Voltage mode control } \rightarrow \Delta B = 1\text{MHz}$

$f_{\text{sw}} = 5\text{MHz}$

Specifications:
- $f_{\text{sw}} = 5\text{MHz}$
- $V_{\text{in}} = 3\text{V}$
- $V_{\text{out}} = 1\text{V}$
- $C_{\text{out}} = 10\mu\text{F}$
- $L = 100\text{nH}$

Output voltage response under load step (2A)

Inductance current response under load step (2A)

- Same voltage drop.
- 20 times less bandwidth in the proposed control making easier the implementation and integration of the system.
5MHz Design example: Output Impedance

**Fast Loop Effect**

![Graph showing fast and slow loop effects.]

- a) Fast and slow loop open
- b) Fast loop closed and slow loop open

**Slow Loop Effect**

![Graph showing fast and slow loop effects.]

- a) Fast loop closed and slow loop open
- b) Fast and slow loop closed

**V^2L_C Control**