Proyecto Fin de Máster

Optimum design of an Envelope Tracking Buck converter for RF PA using GaN HEMTs

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Chapter1. Introduction

I. Motivation for the project

In the modern world of communications today, the demand for broadband and wireless services is growing on a daily basis. This growth directly implies the development of the networks that have to provide these services and one of the problems is their energy consumption. On the other hand, communication today has become very demanding regarding the transmitted data. In order to achieve high quality voice and video transmitting, it is necessary to have a wide bandwidth of the devices which are employed in a signal transmission. This means that there are two goals in the development of these transmission systems: the first one is efficiency improvement and the second one is the enhancement of the complex signal transmission quality which implies high bandwidth of the system. These two requirements are contradictory and present the real challenge from the engineering point of view. This was the motivation for the project presented in this thesis.

II. Introduction to Radio Frequency Power Amplifier

As it was previously mentioned, modern communications today have a wide range of applications, from everyday cell phone and internet services to space and military applications. The radio frequency power amplifier (RFPA) plays a crucial role in the wireless communication system, which has to amplify and reproduce the electric signals in order to transmit them. There are two main features of this PA: linearity and efficiency and there are contradictory in terms of fulfillment. Which feature is dominant, depends on the modulation of the transmitted signal that is applied. Some simple signal modulations like Frequency Modulation (FM) or Frequency Shift Keying (FSK) with constant envelope do not need a linear amplifier and therefore high linearity is not the dominant feature. On the other hand, high linearity is very important when the applied techniques include both amplitude and phase modulation of the input signal, such as Quadrature Phase Shift Keying (QPSK) and Quadrature Amplitude Modulation (QAM).

Also, modern radio techniques based on CDMA (Code Division Multiple Acces), WCDMA (Wide Code Division Multiple Acces), EDGE (Enhanced Data rate for GSM Evolution), WiMAX (Worldwide Interoperability for Microwave Access) and LTE (Long Term Evolution towards 4G data technologies) use envelopes that vary in time. This time variable envelopes in a combination with phase modulation directly require linear PA (class A, B or AB) which suffers from low efficiency. The efficiency of the power conversion in the case of signals with very high Peak-to-Average Ratio (such as WCDMA), if the linear PA, is applied is limited to less than 25% [1]. These high PAR signals require the signal to be decreased significantly from the peak power level of the PA resulting in very poor efficiency.

There are a lot of techniques that are used in order to enhance the efficiency of Radio Frequency Power Amplifier, but two of them are mostly exploited lately: Envelope Tracking (ET) [2] and Kahn's Technique or Envelope Elimination and Restoration (EER) Technique [3] and will be presented in the following section.

III. Mostly exploited efficiency enhancement techniques – ET and EER

Both techniques are based on the voltage modulation at the output of the power supply for RF PA (Figure 1, 3). The main difference between these techniques is the fact that in the case of Envelope Tracking, applied RF PA is linear while in the case of Elimination and Restoration (also known as Kahn's technique), nonlinear power amplifier is used. The converter that supplies the energy is the Envelope Amplifier and is the key component in the signal transmission, regarding the overall efficiency and the bandwidth.

III.1 Envelope Tracking technique

As it was previously mentioned, Envelope Tracking is a technique that requires the supply voltage of RF PA stage to be modulated dynamically with the envelope of the input signal. This would make the PA operate closer to the peak level at all times and dramatically improve the efficiency of the PA. Although implementation difficulties (accuracy, bandwidth, noise, time delay constraints) have made this method impractical in the past, recent improvements in power supply modulation, and the introduction of the High Accuracy Tracking (HAT) supply voltage modulator from Nujira have allowed practical realization of this technique [4].

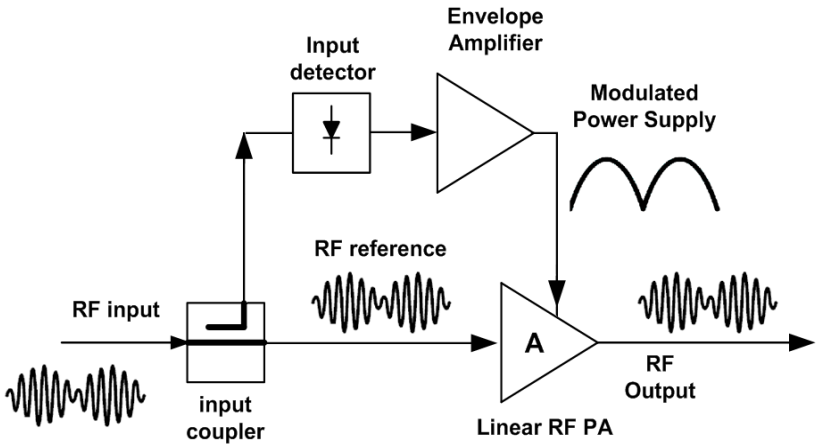

Figure 1:Block schematic based on Envelope Tracking

In this technique, the envelope and phase modulation are done through the linear RF PA while the supply voltage is varied just in order to save energy. The efficiency of the transmitter that uses this technique is significantly better than in the case of a linear RF PA that is supplied from a constant power supply (Figure 2) but still lower than the theoretical efficiency of the Kahn's technique transmitter.

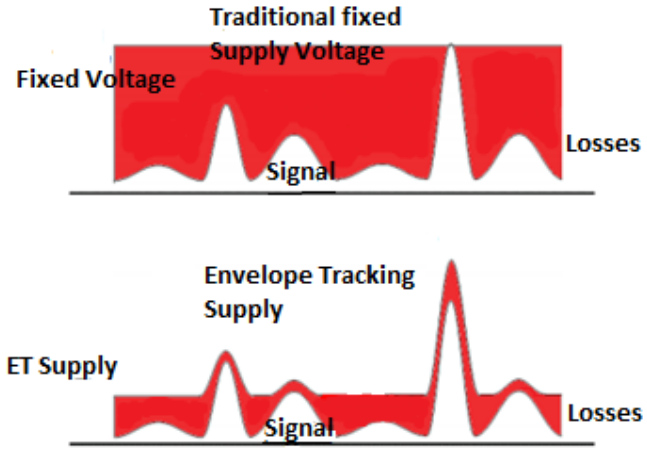

Figure 2:Traditional Supply vs Envelope Tracking Supply

III.2 EER technique

The envelope elimination and restoration (EER) technique was proposed by L. R. Kahn in 1952 as a method for implementing efficient, high power single-side-band (SSB) transmitters and is also referred to as the Kahn method [5]. The block diagram representation of an EER transmitter is shown in Figure 3. A modulated RF signal is split into its polar components; amplitude (envelope) and phase (constant amplitude but phase modulated) signals, by an envelope detector and a limiter respectively. The limiter output is a constant envelope signal that can be amplified by a power efficient but very non-linear switching power amplifier (PA), ideally, without adding significant amplitude (AM/AM) and phase (AM/PM) distortion. The envelope information is restored at the output by modulating the supply voltage of the amplifier, where the modulating signal is derived from the envelope detector.

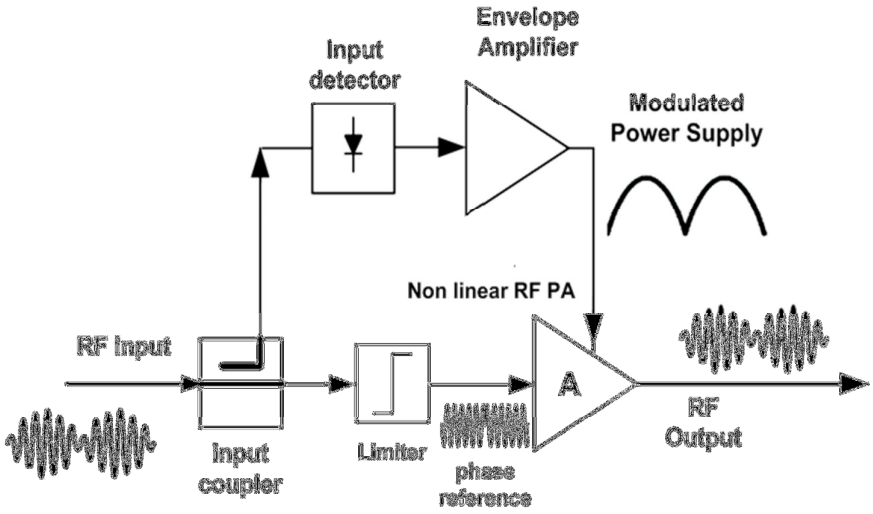

Figure 3: Block schematic of a transmitter based on EER technique

As it can be seen, the total efficiency of the transmitter based on the Kahn's technique is, approximately, the efficiency of the envelope amplifier multiplied by the efficiency of the nonlinear RF PA. The nonlinear RFPA such as Class E usually have efficiency over than 90%. If high efficiency of the envelope amplifier can be obtained, Kahn-technique transmitter can achieve significantly higher efficiency comparing to the ET technique.

IV. Objectives of the project

In this thesis, envelope amplifier for Envelope Elimination and Restoration is designed. This Envelope Amplifier should have fast dynamic response, high efficiency and minimal interference with the output spectrum of the transmitter. A Synchronous Buck converter which can be used for this purpose, needs to fulfill the following requirements: reference tracking of modulating voltage, high linearity, low phase delay, high efficiency. The bandwidth of the converter, the ripple of the output voltage and the converter's efficiency depend on the selection of the switching frequency and the design of the output filter.

In order to obtain high bandwidth, very high switching frequency is needed. This usually implies high switching losses and low efficiency of the converter. This issue was the main challenge in the design proposed in this thesis: how to design the switching converter with high efficiency and bandwidth at the same time?

The solution that was proposed in this thesis is a simple synchronous buck converter with the emphasis on the switching devices that were used. The applied switching devices are based on new technological solution for power switches – Gallium Nitride High Electron Mobility Transistors. GaN material belongs to the group of Wide Band-Gap (WBG) semiconductors which have superior features over Silicon. These physical properties will be presented in Chapter 2. WBG devices are very promising for high frequency applications, because of good Figure Of Merit (product of on-resistance and gate charge) [6], [7], [8], [9]. New generation of Enhancement mode HEMTs built with Gallium Nitride on Silicon, presents a good replacement for Silicon power MOSFETs, and will be used for the prototype in this project. In the aim of comparison with Si, two prototypes of synchronous buck with Silicon MOSFETs with good values for Figure Of Merit were also made. Measurements for 64QAM and WCDMA signals were done and experimental results showed advantages of GaN HEMTs for this kind of application.

On the other hand, important issue is the output filter design, in order to achieve minimum possible distortion of the envelope reference and high efficiency of the converter. Filter design methodology is also proposed (Chapter 3) in order to fulfill these requirements. Experimental results (Chapter 4) confirmed the proposed filter methodology in the case of

sinusoidal output voltage and provided some important conclusions regarding GaN/Si comparison.

Chapter2. New technological solution for power switches: wide band-gap semiconductor devices

I. Why Wide Band-Gap semiconductors?

The term wide band-gap semiconductors refers to an entire family of materials, including the element semiconductor diamond (C), the IV- IV compound semiconductor silicon carbide (SiC) and III-V compound semiconductors like gallium nitride (GaN) and aluminium nitride(AlN). All of them show a wide band-gap, which means that their crystal bonds are stronger than in silicon and more energy E_g is necessary to break an electron out of the bonds i. e. to cross the band-gap.

The most important physical properties of the WBG semiconductors are: wide band-gap, high electric breakdown field, high saturated drift velocity and high thermal conductivity (GaN is exception in this case). The values for Si, SiC, GaN and diamond are presented in Table 1.

Property	Si	6H-SiC	GaN	Diamond
Band-gap, E_g [eV]	**1.12**	**3.03**	**3.45**	**5.45**
Dielectric constant, ε_r	**11.9**	**9.66**	**9**	**5.5**
Electric breakdown field, E_c [kV/cm]	**300**	**2500**	**2000**	**10000**
Electron mobility, μ_n [cm^2/Vs]	**1500**	**500**	**1250**	**2200**
Hole mobility, μ_p [cm^2/Vs]	**600**	**101**	**850**	**850**
Thermal conductivity, λ [W/cmK]	**1.5**	**4.9**	**1.3**	**22**
Saturated electron drift velocity, v_{sat} [x10^7cm/s]	**1**	**2**	**2.2**	**2.7**

Table 1: Physical characteristics of Si and major WBG semiconductors

I.1 Wide band-gap

In a solid, electrons exist at energy levels that combine to form energy bands [10]. A simplified energy band diagram is shown in Figure 4. The top band is called the conduction band and the next lower one is called the valence band. The region between the valence band and the conduction band is called forbidden band, where, ideally, no electrons exist.

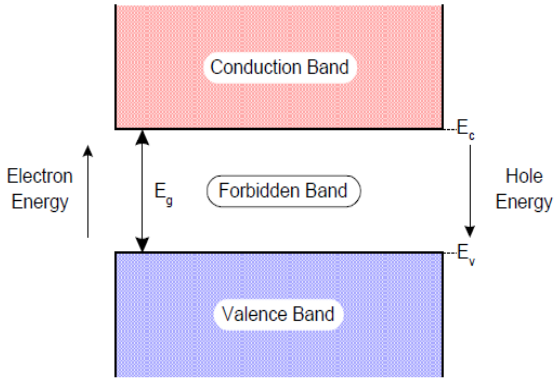

Figure 4: Simplified energy band diagram of a semiconductor

If the electrons in the valence band are excited externally, they can move to the conduction band. In the valence band, they have energy of E_v. In order to move to the conduction band, they need an $E_g = E_c - E_v$. amount of energy, where E_g is the band-gap.

For a conductor like copper, the forbidden band does not exist, and the energy bands overlap. For an insulator, on the other hand, this band is so wide that the electrons need a lot of energy to move from the valence band to the conduction band. In the case of semiconductors, the forbidden band is smaller than for an insulator. WBG semiconductors have very important advantage of the high temperature operation, because of their wider energy band-gap. As the temperature increases, the thermal energy of the electrons in the valence band increases. At a certain temperature, they have sufficient energy to move to the conduction band. This is uncontrolled conduction that must be avoided. The temperature at which this happens is around 150°C for Si. For WBG semiconductors, the band-gap is higher, therefore, electrons in the valence band need more thermal energy to move to the conduction band.

The previous explanation can be presented using the equations for intrinsic carrier concentration.

The intrinsic carrier concentration, n_i, is the number of electron hole pairs in a given semiconductor per unit volume at equilibrium. It is a function of E_g by

$$n_i = \sqrt{N_C N_V}\,\exp(-E_g/2kT) \tag{1}$$

where

$$N_C = 2\left(\frac{2\pi m_e kT}{\hbar^2}\right)^{3/2} \tag{2}$$

and

$$N_V = 2\left(\frac{2\pi m_h kT}{\hbar^2}\right)^{3/2} \tag{3}$$

In the previous equations, m_e and m_h are the effective mass of an electron and hole, respectively. It can be assumed that $m_e = m_h$, thus,

$$n_i = 2\left(\frac{2\pi kT}{2\pi\hbar^2}\right)^{3/2}\exp(-E_g/2kT) \tag{4}$$

As the band-gap increases, the carrier concentration begins to reduce drastically as desired.

The wide band-gap also decreases leakage currents in the switching device. Because leakage currents are proportional to the intrinsic carrier concentration (n_i) or to square of intrinsic concentration (n_i^2), from the previous equations it can be seen that wide band-gap devices provide reduction of leakage currents for several orders of magnitude, comparing to silicon [10]. This is very important feature of the switching device.

The conclusion regarding the wide band-gap is that WBG semiconductors can withstand more heat without losing their electrical characteristics and provide lower leakage currents. They can be used in more extreme conditions where Si based devices cannot be used.

I.2 High critical electric field

Wider band-gap means a larger electric breakdown filed, E_c. A higher electric breakdown field results in power devices with higher breakdown voltages. With high E_c, much higher doping levels can be achieved, thus, device layers can be made thinner at the same breakdown voltage levels. This implies that WBG-semiconductor-based power devices are thinner than their Si based counterparts and have smaller drift region resistances - on resistances. This implies lower conduction losses of the device.

For example, the breakdown voltage (V_B) of a pn diode is expressed as follows [10]:

$$V_B \approx \frac{\varepsilon_r E_C^2}{2qN_d} \tag{5}$$

where q is the charge of an electron and N_d is the doping density.

Using the semiconductor parameters in Table 1, this expression can be simplified as follows:

$$V_B^{Si} \approx \frac{2.96x10^{17}}{N_d} \tag{6a}$$

$$V_B^{4H-SiC} \approx \frac{135x10^{17}}{N_d} \tag{6b}$$

$$V_B^{GaN} \approx \frac{99.4x10^{17}}{N_d} \tag{6c}$$

$$V_B^{diamond} \approx \frac{1519.2x10^{17}}{N_d} \tag{6d}$$

As it can be seen from the previous equations, the theoretical breakdown voltage of a diamond diode is 514 times more than that of a Si diode. For 4H-SiC and GaN, these numbers are 46 and 34 times, respectively. With a higher E_c, more doping can be applied to the material, further increasing the difference between the upper breakdown voltage limits of WBG semiconductors compared to Si.

Another consequence of the higher electric breakdown field and the higher doping density is the width reduction in the drift region. The required width of the drift region can be expressed as [10]:

$$W(V_B) \approx \frac{2V_B}{E_C} \tag{7}$$

Using the electric breakdown field values from Table 1, the drift thickness of the drift region can be calculated:

$$W_d^{Si} = 6.67x10^{-6}V_B \tag{8a}$$

$$W_d^{4H-SiC} = 0.91x10^{-6}V_B \tag{8b}$$

$$W_d^{GaN} = 1x10^{-6}V_B \tag{8c}$$

$$W_d^{diamond} = 0.2x10^{-6}V_B \tag{8d}$$

Diamond, as expected, requires the minimum width, while SiC and GaN follow the diamond in the order of increasing widths.

The last device parameter to be calculated from the properties in Table 1 is the on-resistance of the drift region, which is given by [10]:

$$R_{on} = \frac{4V_B^2}{\varepsilon_S E_C^3 \mu_n} \tag{9}$$

where V_B is the breakdown voltage,

ε_S is the dielectric constant,

E_C is the electric breakdown field and

μ_n is the electron mobility.

The calculation results for on-resistance are plotted in Figure 5, with respect to the breakdown voltage of the device. Again, diamond shows the best performance with SiC and GaN following in increasing order of resistance. The on-resistance of the drift region for the Si device is approximately 10 times more than for the SiC and GaN devices. As the breakdown voltage increases, more doping can be applied to the WBG semiconductors than to Si, so the specific on-resistance ratio between Si and WBG semiconductors increases further.

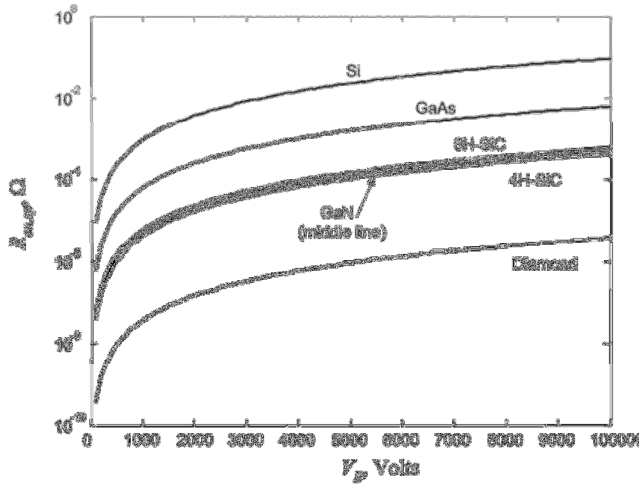

Figure 5: Resistance of the drift region for each material at different breakdown voltages.

I.3 High saturated drift velocity

The high-frequency switching capability of a semiconductor material is directly proportional to its drift velocity. The drift velocities of WBG materials are more than twice the drift velocity of Si ($1x10^7$). Therefore, it is expected that WBG semiconductor-based devices could be switched at higher frequencies than their Si counterparts. Moreover, higher drift velocity allows charge in the depletion region of a diode to be removed faster. Therefore, the reverse recovery current of WBG semiconductor-based diodes is smaller, and the reverse recovery time is shorter.

I.4 High thermal stability

As explained earlier, because of the wide band-gap, WBG semiconductor-based devices can operate at high temperatures. In addition to this, SiC has another thermal advantage - its thermal conductivity. As seen in the following equation, junction-to-case thermal resistance, $R_{th\text{-}jc}$, is inversely proportional to the thermal conductivity [12]:

$$R_{th-jc} = \frac{d}{\lambda A} \tag{10}$$

where λ is the thermal conductivity, d is the length and A is the cross-sectional area.

Higher thermal conductivity means lower $R_{th\text{-}jc}$, which means that heat generated in SiC-based device can more easily be transmitted to the case, heat sink, and then to the ambient. Thus, material conducts heat to its surrounding easily, and the device temperature increases more slowly. For higher-temperature operation, this is critical property of the material. As seen in the Table 1, diamond still leads the other materials by at least a factor of 5, with the SiC devices as the next best material. GaN has the worst thermal conductivity - even lower than Si.

II. New power switches – GaN High Electron Mobility Transistors

High Electron Mobility Transistor (HEMT) is the fastest transistor currently available on the market and a suitable candidate for microwave and millimeter wave applications. It is a heterostructure device and the unique properties of HEMT are the result of band-gap engineering which creates two dimensional electron gas (2DEG) at the heterointerface [11]. Accumulation of the high density 2DEG is due to the formation of a deep spike-shaped quantum well at the heterojunction where a large conduction-band offset as well as a large discontinuity in the piezoelectric and spontaneous polarization are found [14].

Optimized AlGaN/GaN HEMTs play a vital role in the next generation 3G/4G mobile phone base stations, Wi-max, radars, mixers, oscillators, and attenuators in both commercial and military applications [15]. This follows from the superior material properties (comparing to Silicon) presented in the previous section. Exploitation of these material properties and modern growth techniques lead the device to operate at high switching frequency, minimizing the conduction and switching losses.
Cross section of AlGaN/GaN HEMT is presented in Figure 6. AlGaN is a wide band-gap semiconductor of energy gap, Eg = 4.24 eV while GaN has a comparative less band-gap than AlGaN, Eg = 3.4 eV. The growth of wide band-gap material over narrow band gap material creates a 2DEG in the heterointerface, so that accumulation of electrons in the quantum well is possible, which leads to higher mobility and resulting into high speed device. 2DEG formation and subbands of AlGaN/GaN HEMT are presented in Figure 7.

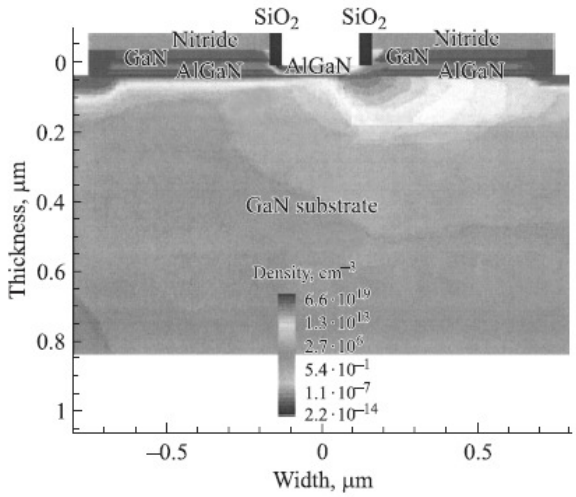

Figure 6: AlGaN/GaN-based HEMT structure

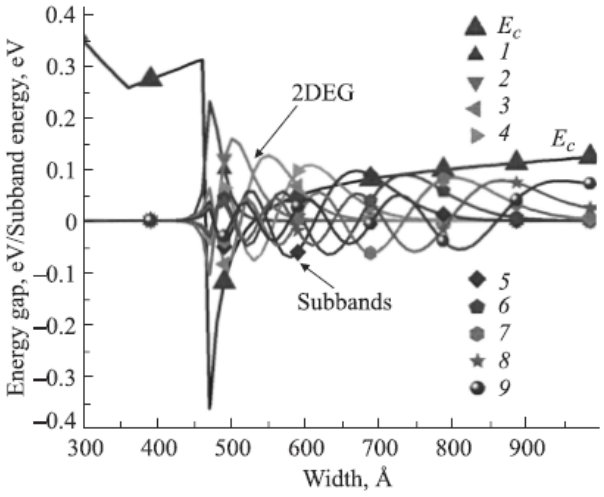

Figure 7: 2DEG and sub bands of AlGaN/GaN-based HEMT

In order to explain 2DEG generation, it is necessary to explicate basics of the polarization effects which are typical for this material.

AlGaN and Gan possess polarized Wurtzite crystal structures, having dipoles across the crystal in the [0001] direction as shown in Figure 8. In the absence of external fields, this macroscopic polarization includes spontaneous (pyroelectric) and strain induced (piezoelectric) contributions

[12], [13], [14], [15]. The primary effect of polarization is an interface charge due to very sharp divergence in the polarization at the AlGaN/GaN heterointerface.

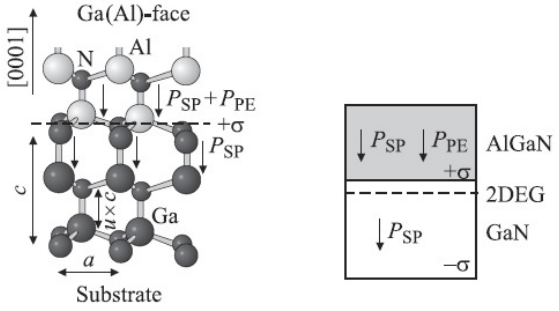

Figure 8: Crystal structure and polarization effects

If we assume that GaN bulk is fully relaxed, its polarization vector contains only the spontaneous component, *P*sp(GaN). But for AlGaN layer, in addition to the spontaneous component *P*sp(AlGaN), the piezopolarization component due to the presence of strain because of Al content in Al*x*Ga1−*x*N must be considered and is shown in Fig. 8. The aforementioned polarization fields result in a higher potential barrier at the backside of the 2DEG which improves the carrier concentration and reduces the buffer leakage. Quantitative analysis of 2DEG can be realized by solving Schrodinger's wave equation [10].

The large polarization divergence at the Al*x*Ga1−*x*N barrier surface would completely deplete the channel of electrons, if not partially or completely compensated by positive charges. It is still not clear to the research community, whether the polarization charge is compensated by fixed charges or by interface trap states. Due to the relatively immature state of III-nitride technology, these materials tend to exhibit a significant number of structural defects, such as threading, misfit dislocations, and carbon impurities, which translate into bulk traps [16–18]. The lack of high quality large substrates is the main reason why vertical GaN HEMTs are not commercially available yet.

III. Technological challenges in GaN domain

Regarding the substrates that were used, GaN HEMTs have been demonstrated on Si, SiC, sapphire and on native GaN substrates.

As it was presented in the previous section, Gallium Nitride material has a low value for thermal conductivity, even lower than Silicon. This fact implies problems with power dissipation which is an important limitation regarding high temperature operation of the device. In order to improve the overall thermal conductivity of the device, Silicon-Carbide can be used as a substrate for GaN HEMT. In that way, high power devices can be fabricated.

On the other hand, sapphire is much cheaper comparing to SiC (more than 10 times) but its thermal conductivity is significantly lower. It can be used as a substrate for low power devices.

However, Si and SiC are the preferred choices for RF devices. The maturity of the AlGaN/GaN heterostructures in terms of reliability on the first place, cost and manufacturability has been demonstrated through the use of commercially available Si substrates. Si substrates have low crystal defect density and offer a high quality surface as required for performing epitaxy process [19]. Additionally, the wafer-wafer consistency and quality are unmatched in other materials and are the result of decades of optimization of the manufacturing process of Si substrates. Due to the relative lack of widespread usage and immaturity of high quality SiC substrates for RF applications, SiC standards for substrates are not established in the open literature.

Besides substrates issues, packaging of GaN HEMTs is also an important question, in order to improve thermal management. In the case GaN HEMTs from EPC that were tested in this project, the active device is isolated from the substrate and fully encapsulated by passivation layers on the front side as shown in Figure 9. This configuration allows EPC's GaN transistors to be used as bare die without additional packaging. The advantages of this technological approach include: the elimination of plastic packages and the related performance issues (for example additional leakage inductance of the package) and cost reduction. On the other hand, the main drawback is worse thermal management caused by the absence of the package.

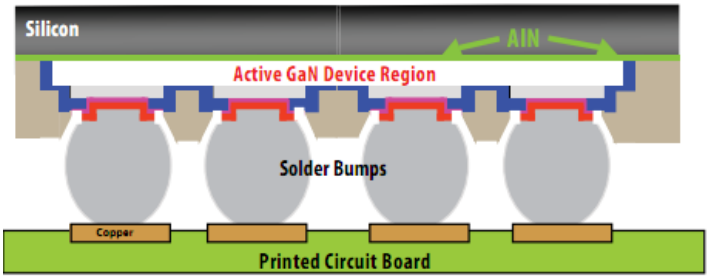

Figure 9: Cross section of GaN HEMT from EPC

Chapter3. Output filter design methodology

I. Switching frequency selection method

The main objectives of the filter design in synchronous buck for RF PA are generation of the envelope reference with minimum possible distortion and high efficiency of the converter. Optimum efficiency point can be obtained by the optimum trade-off between conduction and switching losses.
Regarding the selection of a correct switching frequency, an analysis of the inter-modulation products induced by the PWM on the envelope signal is an important issue. It is assumed that the modulating signal with tone frequency f_{mod} yields duty cycle d(t) in the power stage [20]

$$d(t) = \frac{\alpha}{2}(1 + \sin(2\pi f_{\mathrm{mod}} t)) \tag{11}$$

A single tone modulating signal is used to establish the Fourier series decomposition of the PWM signal at the input of the filter

$$x_{pwm}(t) = \frac{V_{IN}\alpha}{2} + \frac{V_{IN}\alpha}{2}\sin(2\pi f_{\mathrm{mod}} t) + \sum_{n=1}^{\infty}\frac{V_{IN}}{\pi n}\sin(2\pi n f_s t) - \sum_{n=1}^{\infty}\frac{V_{IN}}{\pi n}\sum_{k=\pm 1}^{\pm\infty} J_k(-n\pi\alpha)\sin(2\pi(nf_s + kf_{\mathrm{mod}})t - n\pi\alpha) \tag{12}$$

where J_k is a Bessel function of the first kind.
For a multi-tone like RF envelope, the analysis is very difficult though [21] proposes a method to determine an equivalent single tone. Equation 12 is useful to estimate the effect of PWM noise on the output signal [20]. In particular it shows that PWM spectrum does not contain harmonics contribution of f_{mod}. Also, it shows that most of the noise is concentrated in high frequency range, around the harmonics of the switching frequency. However, some aliasing spurious ($nf_s \pm kf_{mod}$) appear in low frequency range, as PWM is a sampling process and therefore increase the overall near-band noise. In order to minimize both the near-band and the high frequency noise, switching frequency has to be increased so the corresponding spurious frequencies fall in the frequency range where the attenuation of the LC filter is high enough.

Even with high switching frequency, spurious frequencies due to the fourth term of Eq. 12 fall close to the baseband but with very low magnitude since the Bessel functions are scaled by 1/n!.
In order to obtain the desired attenuation of the duty cycle to output voltage transfer function for the filter with resonance frequency equal to f_0, the minimum switching frequency, f_{sw}, is defined as

$$f_{sw} = f_0 10^{\frac{att}{40}} \tag{13}$$

where a_{tt} is a desired attenuation in dB (Figure 10). The resonance frequency of the filter is given by

$$f_0 = \frac{1}{2\pi\sqrt{L_{OUT}C_{OUT}}} \tag{14}$$

In previous equation, C_{OUT} and L_{OUT} are the values for the filter inductor and capacitor. These values will be determined in order to provide the optimum efficiency point by minimizing conduction and switching losses.

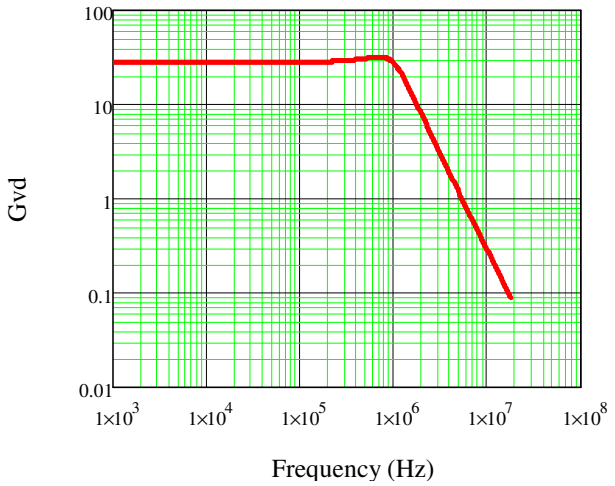

Figure 10: Duty cycle to output voltage transfer function

From the previous analysis, it is obvious that there is a trade-off between the bandwidth and overall efficiency that can be achieved. In order to decrease the overall losses at high switching frequency, it is necessary to minimize

conduction losses and to find the optimum point regarding this trade-off. Filter design methodology that is proposed, provides the aforementioned optimum point, using a power losses model that will be presented in the following section.

II. Power losses model

Power losses model will be derived for a synchronous buck presented in Figure 11 in the case of sinusoidal output voltage.

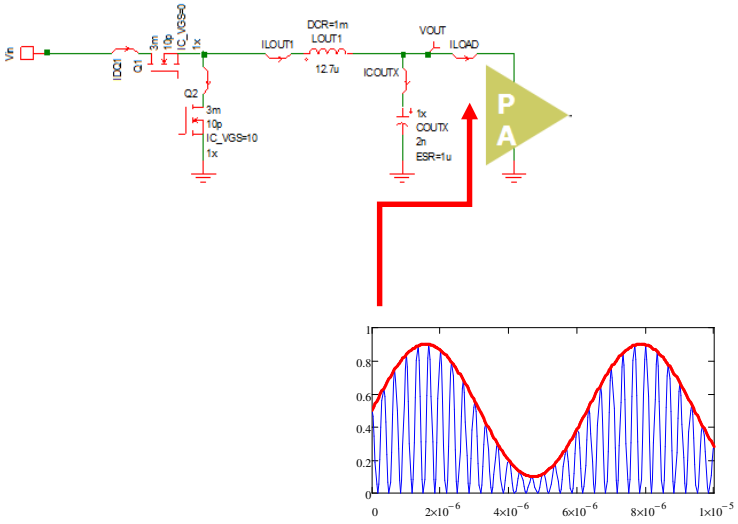

Figure 11: Synchronous Buck for RF PA

Conduction losses for the presented topology are given by the next equations

$$P_{MOS} = R_{DSON} I_{L\_RMS}^2 \tag{15a}$$

$$P_L = R_L I_{L\_RMS}^2 \tag{15b}$$

$$P_C = R_{ESR} I_{C\_RMS}^2 \tag{15c}$$

where R_L, R_{ESR}, R_{DSON} are inductor resistance, capacitor equivalent series resistance and on resistance of a power switch while I_{L_RMS} and I_{C_RMS} present RMS values of inductor and capacitor current, respectively.

Regarding the switching losses, we distinguish high-side and low-side losses.

The switching interval of a high-side switch is broken up into five periods (t_1 to t_5) as illustrated in Figure 12 [22]. The top drawing in Figure 12 shows the voltage across the switch and the current through it. The bottom timing graph represents V_{GS} as a function of time. The shape of this graph is identical to the shape of the Q_G curve contained in MOSFET datasheets, which assumes that gate is being driven with constant current. The notations indicate which Q_G is being charged during the corresponding time period.

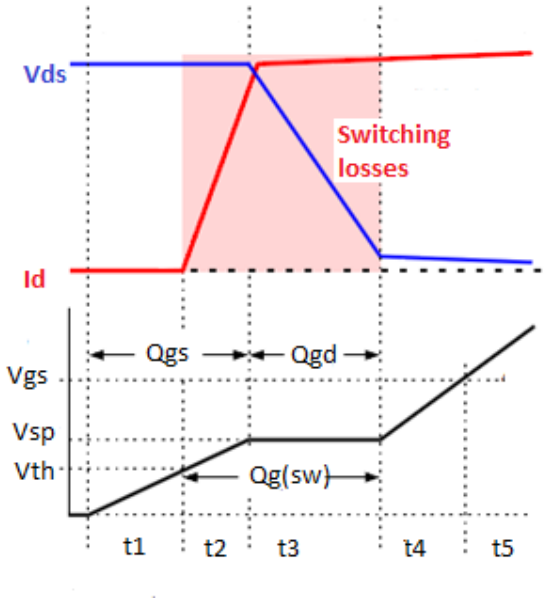

Figure 12: High-Side switching losses and Q_G

The switching interval begins when the high-side MOSFET driver turns on and begins to supply current to high-side's gate to charge its input capacitance. There are no switching losses until V_{GS} reaches the threshold voltage, $V_{TH.}$ Therefore, P_{t1}=0.

When V_{GS} reaches $V_{TH,}$ the input capacitance is being charged and the MOSFET's drain current is rising linearly until it reaches the inductor current. During this period (t_2), the switch is sustaining the entire input voltage across it, therefore, the energy in the MOSFET during t_2 is:

$$E_{t2} = t_2 \frac{V_{IN} I_{LAVG}}{2} \tag{16}$$

where I_{LAVG} is the average value of the inductor current.

During the next time interval, t_3, inductor current is flowing through high-side switch and the drain-to-source voltage begins to fall. Now, all of the gate current will be going to recharge the capacitance between gate and drain, C_{GD}. During this time interval, the voltage is falling linearly from V_{IN} to 0. Therefore:

$$E_{t3} = t_3 \frac{V_{IN} I_{LAVG}}{2} \tag{17}$$

During t_4 and t_5, the switch is just fully enhancing the channel to obtain its rated on-resistance at a rated V_{GS}. The losses during this time are very small comparing to the ones in t_2 and t_3, so we can ignore them in the analysis.

From (16) and (17), for the main part of high-side switching losses, we obtain:

$$P_{SW\_HS} = \frac{V_{IN} I_{LAVG}}{2} (t_2 + t_3) f_{SW} \tag{18}$$

Time intervals t_2 and t_3 are determined by the driver capability to deliver all of the charge required in that time period:

$$t_x = \frac{Q_{G(x)}}{I_{DRIVER}} \tag{19}$$

where x=2,3.

Most of the switching interval is spent in t_3, which occurs at a voltage that is referred as a "switching point" or V_{SP}. This voltage can be approximately calculated as:

$$V_{SP} \approx V_{TH} + \frac{I_{LAVG}}{G_M} \tag{20}$$

where G_M is the MOSFETs transconductance and V_{TH} is its typical gate threshold voltage.

Regarding the calculation of the driver current, it is necessary to separate the rising time (L-H) and falling time (H_L), since this current can be different for each edge:

$$I_{DRIVER(L-H)} = \frac{V_{DD} - V_{SP}}{R_{DRIVER(PULL-UP)} + R_{GATE}} \tag{21}$$

$$I_{DRIVER(H-L)} = \frac{V_{SP}}{R_{DRIVER(PULL-DOWN)} + R_{GATE}} \tag{22}$$

where V_{DD}, $R_{DRIVER(PULL-UP)}$, $R_{DRIVER(PULL-UP)}$ are voltage supply of the driver, its resistance during the rising and the falling edge, respectively, while R_{GATE} is the gate resistance of the switch.

The V_{GS} excursion during t_2 is from V_{TH} to V_{SP}. Approximating this as V_{SP} simplifies the calculation considerably and introduces no significant error. This approximation also allows us to use the $Q_{G(SW)}$ term to represent the gate charge for a MOSFET, which is moved within a switching interval. Approximately, this charge can be determined as:

$$Q_{G(SW)} \approx Q_{GD} + \frac{Q_{GS}}{2} \tag{23}$$

Therefore, the expressions for the switching times are:

$$t_{S(L-H)} \approx \frac{Q_{G(SW)}}{I_{DRIVER(L-H)}} \tag{24}$$

$$t_{S(H-L)} \approx \frac{Q_{G(SW)}}{I_{DRIVER(H-L)}} \tag{25}$$

In that way, most of the high-side switching losses can be presented as:

$$P_{SW\_HS} = \frac{V_{IN} I_{LAVG}}{2} (t_{S(H-L)} + t_{S(L-H)}) f_{SW} \tag{26}$$

There are several additional losses that are typically much smaller than the aforementioned losses. The first among them are gate losses of the switch

$$P_{GATE} \approx Q_{GATE} V_{DD} f_{SW} \tag{27}$$

where Q_{GATE} is the gate charge of the switching device, V_{DD} is the supply voltage of the driver and f_{SW} is the switching frequency.

The next one is the power to charge the output capacitance of the switch:

$$P_{COSS} \approx \frac{C_{OSS} f_{SW} V_{IN}^2}{2} \tag{28}$$

where C_{OSS} is the output capacitance of the switch.

Finally, there are power losses due to reverse recovery of the body diode of a low side switch:

$$P_{QRR} = Q_{RR} V_{IN} f_{SW} \tag{29}$$

where Q_{RR} is the body diode's reverse recovery charge.

Low-side switching losses for each edge can be calculated in a similar way. Figure 13 shows low-side turn-on switching loss waveforms while Figure 14 shows low-side turn-off waveforms.

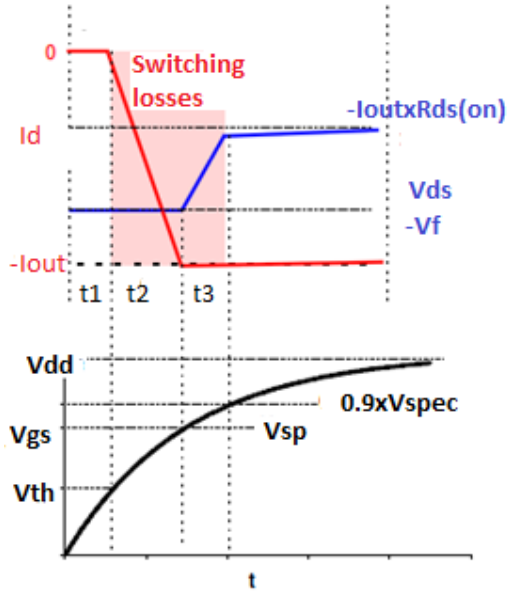

Figure 13: Low-Side turn on switching loss waveforms

From these figures, approximately we obtain:

$$P_{SW(LS)} \approx (t_2 V_F + t_3 \frac{V_F + I_{LRMS} 1.1 R_{DS(ON)}}{2}) I_{LRMS} f_{SW} \tag{30}$$

If we make comparison with expression (26) for high-side switch, we conclude that instead of V_{IN}, we use the forward voltage drop on the body diode, V_F. Also, there is almost no Miller effect for the low-side MOSFET, since V_{DS} is increasing (becoming less negative) as we turn the device on. At

the end of time interval t_3, V_{GS} is equal to 90% of V_{SPEC}. For this value, $R_{DS(ON)}$ is typically 110% of the specified $R_{DS(ON)}$.

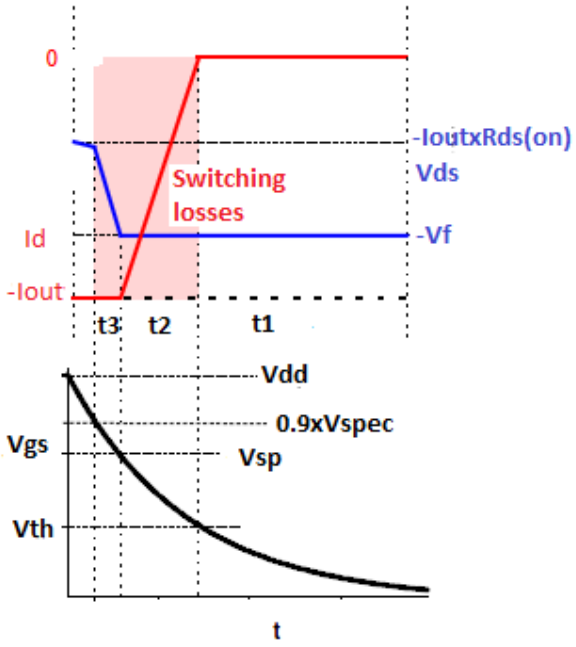

Figure 14: Low-Side turn off switching loss waveforms

The rising edge transition times for the low-side switch, t_{2R} and t_{3R}, can be calculated in the following manner

$$t_{2R} = K_{2R}(R_{DRIVER} + R_{GATE})C_{ISS} \tag{31}$$

where

$$K_{2R} = \ln\left(\frac{V_{DD}}{V_{DD} - V_{SP}}\right) - \ln\left(\frac{V_{DD}}{V_{DD} - V_{TH}}\right), \tag{32}$$

while V_{DD} and R_{DRIVER} present the driver voltage supply and resistance, respectively.

For t_{3R} we obtain:

$$t_{3R} = K_{3R}(R_{DRIVER} + R_{GATE})C_{ISS} \tag{33}$$

where

$$K_{3R} = \ln(\frac{V_{DD}}{V_{DD} - 0.9V_{SPEC}}) - \ln(\frac{V_{DD}}{V_{DD} - V_{SP}}) \cdot \tag{34}$$

In the previous equations, C_{ISS} presents input capacitance of the low-side switch, when V_{DS} is close to zero.

The falling edge transition times for the low-side switch, t_{2F} and t_{3F}, can be calculated in a similar way

$$t_{3F} = K_{3F}(R_{DRIVER} + R_{GATE})C_{ISS} \tag{35}$$

$$t_{2F} = K_{2F}(R_{DRIVER} + R_{GATE})C_{ISS} \tag{36}$$

where

$$K_{3F} = \ln(\frac{0.9V_{SPEC}}{V_{SP}}) \tag{37}$$

$$K_{2F} = \ln(\frac{0.9V_{SPEC}}{V_{SP}}) \cdot \tag{38}$$

In addition to previously defined losses, it is necessary to mention and define dead-time or body-diode conduction losses.

The dead time is the amount of time during which both MOSFETs are off. During this time, body-diode of the low-side switch is in forward conduction. It's power losses can be defined as

$$P_{DEAD\_TIME} = t_{DEAD\_TIME} I_{LAVG} V_F f_{SW} \tag{39}$$

where V_F is a body-diode forward voltage while t_{DEAD_TIME} can be determined as

$$t_{DEAD\_TIME} = t_{DEAD\_TIME(R)} + t_{DEAD\_TIME(F)} \tag{40}$$

$t_{DEAD\_TIME\ (R)}$ and $t_{DEAD\_TIME(F)}$ are the dead times associated to the periods before the voltage at the input of the filter rises, after low-side turns off, and after the voltage falls, before low-side turns on, respectively.

During the $t_{DEAD\_TIME(F)}$, the body-diode is conducting the full load current from the time when node at the input of the filter falls, until the low-side switch reaches threshold. This dead time consists of two parts: $t_{DELAY(F)}$ - the driver's built in delay and t_{TH} - the time that driver needs to charge the low-

side MOSFET's gate to reach the threshold voltage, V_{TH}. t_{TH} can be approximated by:

$$t_{TH} \approx \frac{Q_{GS}}{2I_{LDRV}} \tag{41}$$

In order to make the previous approximation acceptable, it is necessary to assume that before reaching the threshold, the gate voltage is low enough so I_{LDRV} can be approximated with a constant current:

$$I_{LDRV} \approx \frac{V_{DD} - (\frac{V_{TH}}{2})}{R_{GATE} + R_{DRIVER}} \tag{42}$$

while Q_{GS} is typically

$$Q_{GS} \approx 2Q_{G(TH)} \tag{43}$$

From (41), (42) and (43) we obtain

$$t_{DEAD\_TIME(F)} = t_{DELAY(F)} + \frac{Q_{G(TH)}(R_{GATE} + R_{DRIVER})}{(V_{DD} - \frac{V_{TH}}{2})} \tag{44}$$

$t_{DEAD\_TIME\ (R)}$ can be calculated in a similar way:

$$t_{DEAD\_TIME(R)} = t_{DELAY(R)} + t_{SP} \tag{45}$$

where $t_{DELAY(R)}$ is the driver's built in delay and t_{SP} is the time it takes for the high-side MOSFET's gate to charge to V_{SP}:

$$t_{SP} \approx \frac{Q_{G(SP)}(R_{GATE} + R_{DRIVER})}{(V_{DD} - \frac{V_{SP}}{2})} \tag{46}$$

III. Proposed methodology for the filter design

Using the power losses model presented in the previous section, filter design methodology will be proposed, with the aim of optimum efficiency point determination.

Analyzing the circuit from Figure 11, we obtain that the inductor-to-load current ratio is given by:

$$\frac{i_L}{t_{LOAD}} = 1 + R_{LOAD} C_{OUT} s \tag{47}$$

and it's frequency dependence is presented in Figure 15 .

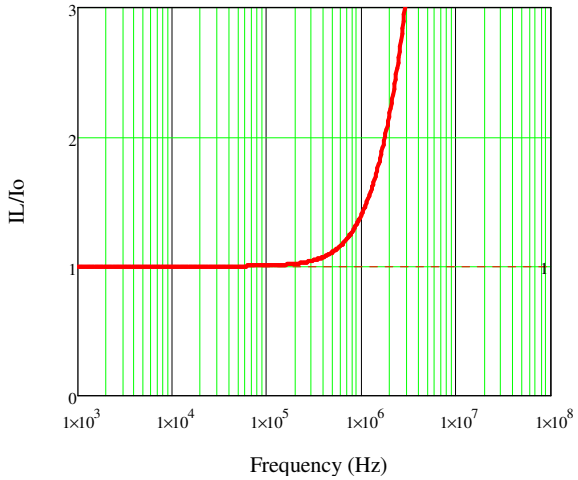

Figure 15: Frequency dependence of inductor to load current ratio

If we select the frequency equal to the frequency of the output modulated voltage, we obtain:

$$\frac{i_{L\max}}{t_{LOAD\max}} (j 2\pi f_{MOD}) = A \tag{48}$$

where A is the design parameter which always complies the condition:

$$A \geq 1 \tag{49}$$

and i_{Lmax}, $i_{LOADmax}$ are the maximum values of the inductor and load current, respectively. Assuming that the ratio of these maximum values is set to A, for C_{OUT} we obtain:

$$C_{OUT} = \frac{\sqrt{A^2 - 1}}{2\pi f_{MOD} R_{LOAD}} \tag{50}$$

Higher values for C_{OUT} correspond to higher values of A which means that inductor-to-load current ratio is higher. This directly implies higher conduction losses.

Minimization of C_{OUT} provides lower conduction losses but increases a corner frequency of the filter. This implies the higher switching frequency for the same attenuation value and higher switching losses. In order to decrease the corner frequency of the filter, we choose the maximum value for the inductance $L_{OUT.}$

The criteria for L_{OUT} determination is to avoid duty cycle saturation. From duty cycle-to-output voltage transfer function, $G_{vd}(s)$, we obtain:

$$d(s) = G_{vd}^{-1}(s) v_{OUT}(s) \tag{51}$$

where $d(s)$ (Figure 16) and $v_{OUT}(s)$ present the duty cycle and the output voltage in the frequency domain.

If the maximum change of the output voltage, Δv_{OUT}, corresponds to the maximum change of the duty cycle, $\Delta d=1$, we obtain:

$$\frac{\Delta v_{OUT}}{v_{IN}} \sqrt{[1 - L_{OUT} C_{OUT} (2\pi f_{MOD})^2]^2 + \frac{L_{OUT}}{R_{LOAD}} (2\pi f_{MOD})^2} = 1 \tag{52}$$

where V_{IN} is the input voltage of the converter, R_{LOAD} is the output resistance and f_{MOD} is the frequency of the output voltage. Solving the previous equation we obtain the value for L_{OUT}.

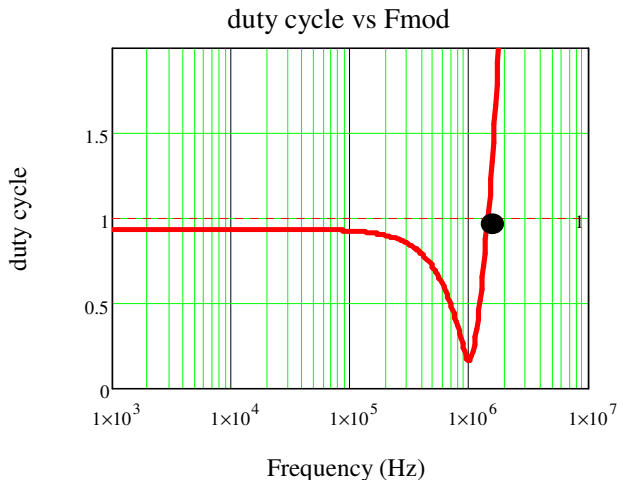

Figure 16: Frequency dependence of the duty cycle

If we implement the power losses model (presented in the previous section) in Matlab, we obtain the losses dependence on the filter design parameter A. The mean value of the inductor current was calculated using the number of samples which is equal to the ratio of the switching frequency and frequency of the output voltage, f_{SW}/f_{MOD}. Figure 17 presents the efficiency dependence of a synchronous buck converter on the filter design parameter A. The results from Figure 17 are obtained for the converter with the following specifications:

- Input voltage is 24V
- Output voltage swing is 20V
- The load resistance is 15Ω
- Frequency of the modulated sine wave is 200kHz.
- Desired attenuation of the filter is 47dB
- The transistor that was analyzed was EPC1015 GaN HEMT.

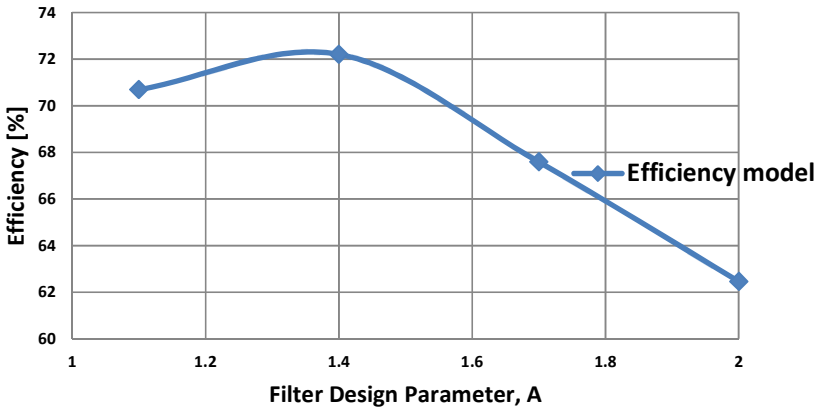

Figure 17: Efficiency model for different filter designs for R=15Ω

Analyzing the curve in Figure 17, it can be seen that for A approximately equal to 1.4, efficiency has the highest value, i. e. this point corresponds to the optimum efficiency point.

If the value for the output resistance, R_{LOAD}, is decreased to 6Ω, with the same specifications regarding the input voltage, output voltage, frequency of the modulated sine wave and desired attenuation of the filter, the efficiency dependence is different (Figure 18) and the optimum point is shifted to the lower value of A and higher switching frequency. In a similar manner, if the R_{LOAD} is changed to the higher values (30 Ω and 100 Ω), the optimum point is shifted to the higher values of design parameter A and lower switching frequency. This behavior is quite expected: for higher values of the load, the optimum efficiency point corresponds to the higher switching frequency and switching losses, in order to "decrease" conduction losses which are dominant for high currents. On the other hand, for lower values of the load, optimum value for A is shifted to the higher values which are increasing conduction losses, because these losses are not dominant for low currents. In this way, we make optimum "balance" between conduction and switching losses, depending on the load.

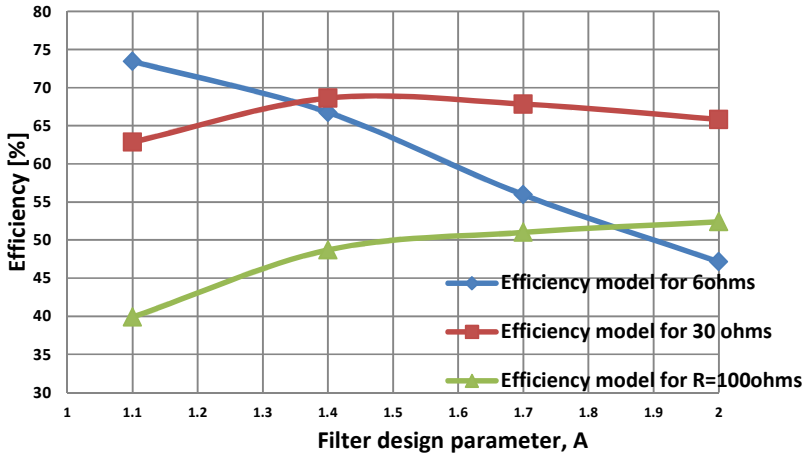

Figure 18: Efficiency model for different filter designs for R=15Ω, 30 Ω and 100 Ω

The proposed filter design methodology for sinusoidal output voltage, will be verified through the experimental results.

In order to apply this methodology for RF signals, it is necessary to develop power losses model for random signals.

Chapter4. Experimental results

Regarding the optimum design of an envelope tracking buck converter for RF PA, experimental results verified the proposed filter design methodology and on the other hand showed advantages of GaN High Electron Mobility Transistors comparing to Si MOSFETs.

Filter design methodology was verified for sinusoidal output voltage, using four different filter designs. Obtained experimental results showed good correspondence with the model regarding the optimum efficiency point determination.

In order to make comparison between new technological solution for power switches based on Gallium Nitride and standard Silicone devices, three prototypes of synchronous buck were made. Static efficiency measurements were made as well as dynamic tests with 64QAM and WCDMA signals. Obtained results showed the highest efficiency of GaN prototype in a low power range which is our goal in the case of envelope amplifier.

I. Filter design methodology verification

In order to demonstrate the optimum efficiency point determination, four filter designs were made for four different values of parameter A.

For V_{IN}=24V and R_{LOAD}=15Ω, sinusoidal output voltage of 200kHz with the voltage swing of 21V was generated, using the prototype with GaN HEMTs. Obtained results are presented in Table 2. As it was previously mentioned, lower A values correspond to higher switching lossess and higher A values to higher conduction losses. Experimental results showed good correspondence with the power losses model, regarding the determination of the optimum efficiency point (Figure 19) which is found for A around 1.4, in the case of 15Ω of the output resistance. Still, there is an offset between the predicted and obtained efficiency values, which demands an improvement of the power losses model. For A=1.4, output voltage waveform is presented in Figure 20.

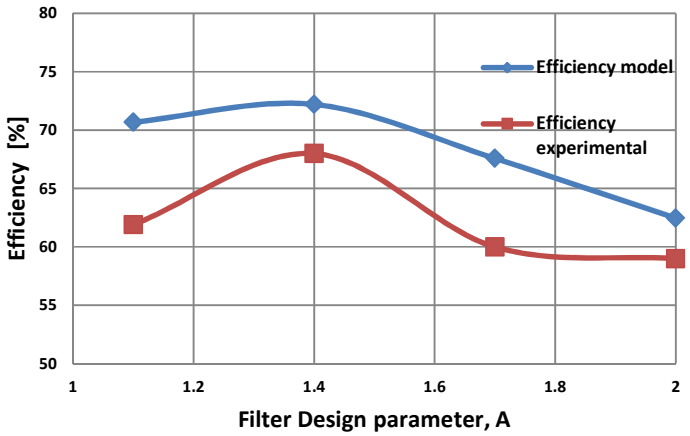

Figure 19: Comparison of efficiency model and experimental results for different filter designs, for R=15Ω

	A = 1.1	A =1.4	A = 1.7	A = 2.0
f_{SW}[MHz]	5.9	4.2	3.7	3.5
L[uH]	8.7	8.9	8.1	7.4
C[nC]	18	40	56	66
P_{LOSSES}[W]	5.6	4.9	6.9	8.3

Table 2: Comparison of four different filter designs for the average output power of 10W

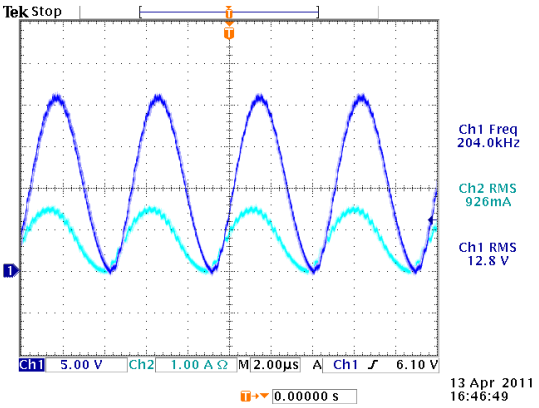

Figure 20: Sinusoidal output voltage (dark blue) and inductor current (light blue) for A=1.4

II. Comparison of GaN and Si devices

II.1 Figure Of Merit

As it was already explained in Chapter 2, new generation of GaN devices is very promising for high switching frequency applications. In order to make comparison between different devices for the same specifications, we use the Figure Of Merit which is defined as:

$$FOM = Q_G R_{DS(ON)}$$

where Q_G presents the total gate charge of the device while $R_{DS(ON)}$ is on resistance of the switch.

For the same specifications regarding the breakdown voltage and maximum drain current, FOMs for GaN HEMT from EPC and two Si MOSFETs from Infineon [24] are presented in Table 3. These Si devices were selected because of their good value for the FOM. Still, it can be seen that EPC1015 has much better FOM than BSC016N04LSG and BSZ097N04LSG, at least for a certain range of frequencies, voltages and power.

Device	Type	V_{ds_max}[V]	R_{on}[mΩ]	Q_G[nC]	FOM
EPC1015	**GaN**	**40**	**3.2**	**11.6**	**37.1**
BSZ097N04LSG	**Si**	**40**	**11.4**	**8.6**	**98.04**
BSC016N04LSG	**Si**	**40**	**1.8**	**54**	**97.2**

Table 3: Characteristics of the switching devices

The devices presented in Table 3 were used for high-side and low-side switch in three different prototypes of a synchronous buck.

The first prototype was made using two EPC1015 GaN HEMTs, two isolation chips from Texas Instruments, ISO721, and two EL7155 drivers from Intersil, while a XILINXs SPARTAN3 FPGA board was used to provide the control signals. The simplified schematic of the topology is presented in Figure 21.

In order to make a comparison with Si MOSFETs, the second and the third prototypes were built using BSZ097N04LSG and BSC016N04LSG Si power transistors from Infineon, with previously calculated values for FOM. All of

the three prototypes were made in the same way, regarding the PCB layout, isolation chips and drivers that were used, in order to make the precise comparison between the performance of GaN and Si devices. The only difference in the PCB layout was the footprint for the switching devices.

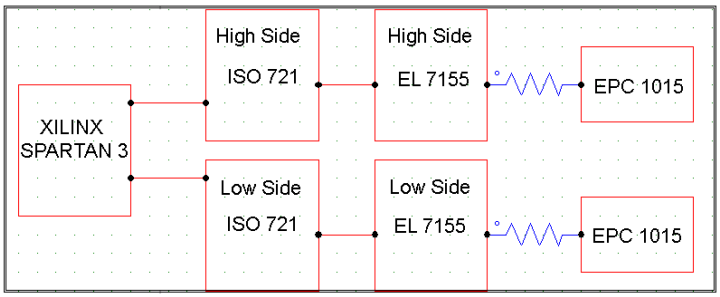

Figure 21: Simplified schematic of a driving circuit with GaN HEMTs

II.2 Packaging influence on operating conditions

The first measurements for all three prototypes were made for a constant output voltage. The drain-to-source voltage waveform of the low-side switch, in the case of both Si MOSFETs showed significantly higher overshoot comparing to the GaN HEMT (Fig. 22 and 23), due to higher leakage inductance of PG-TSDSON-8 Si transistor package. This fact limits the value of the input voltage that can be applied to the Si prototypes. In order to apply 24V at the input of each prototype, it was necessary to put additional resistance in the gate of a high-side Si MOSFETs in order to obtain slower turn-on of a high-side switch and a lower overshoot. Measurements showed that in the case of BSC016N04LSG it was enough to add 1.5Ω in the gate while in the case of BSZ097N04LSG, 3.3 Ω was added in order to achieve safe operating conditions with 24V at the input.

Device	Type	V_{IN}[V]	R_gate_additional[Ω]
EPC1015	**GaN**	**24**	**-**
BSZ097N04LSG	**Si**	**24**	**3.3**
BSC016N04LSG	**Si**	**24**	**1.5**

Table 4*: Additional gate resistances in order to achieve safe operating conditions for 24V at the input*

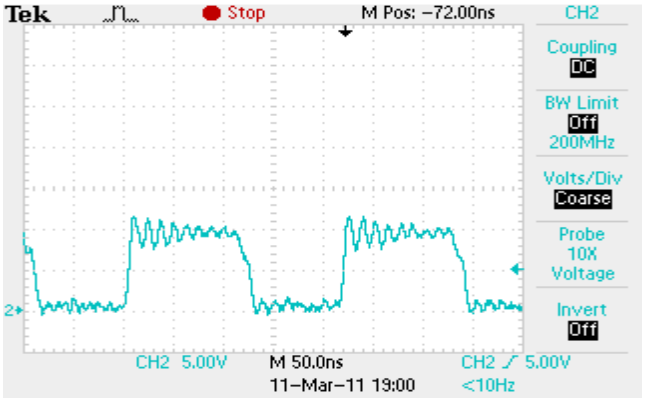

Figure 22: Measured Vds of the low-side switch in GaN prototype for Vin=10V

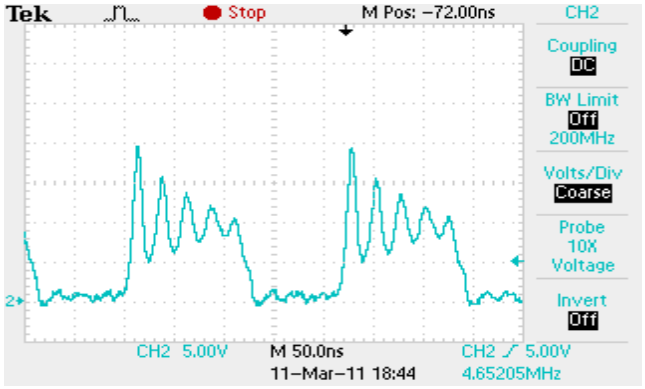

Figure 23: Measured Vds of the low-side switch in prototype with BSZ097N04LSG MOSFETs for Vin=10V

On the other hand, GaN HEMTs from EPC cannot provide so good thermal management as presented Si MOSFETs from Infinieon. Problems with power dissipation make the comparison regarding packaging relative: Si MOSFETs that were tested do have package with higher leakage inductance which demands additional gate resistance but can provide better thermal management for higher output power. In order to make this comparison correct, it is necessary to wait for GaN HEMTs with more "mature" packaging.

II.3 Static characteristics

The first efficiency measurements for each prototype were made for a constant output power, at switching frequency equal to 4.7MHz, changing the value for the duty cycle in order to provide different power levels at the output. For input voltage equal to 24V and output resistance of 6Ω, duty cycle was changed from 30% to 70%. The efficiency measurements were made in this manner because in RF application, the output voltage of the converter tracks the RF reference by the modulation of the duty cycle, while the load resistance is being constant (RF PA behaves as a purely resistive load).

The efficiency measurements for all three prototypes are presented in Figure 24. The prototype with GaNs showed the highest efficiency in the low power range (up to 25W). Low power is the goal in the case of Envelope Amplifier, because of the high peak-to-average power ratio (PAPR) of the transmitted signals, such as WCDMA.

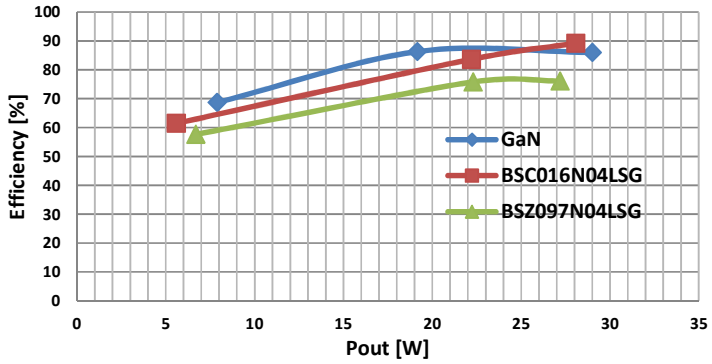

Figure 24: Efficiency measurement for all three prototypes at 4.7MHz for R_{LOAD} =6 Ω

II.4 Dynamic tests: implementation of 64QAM and WCDMA signals

Before we present the results obtained for WCDMA and 64QAM waveforms at the output of the converter, we have to define operating conditions for all three prototypes.

In order to track RF signals, it is necessary to provide duty cycle generation from almost 0% to almost 100%. If the switching frequency is around 5MHz,

it means that it is necessary to have drivers with very low built-in (intrinsic) delay. Otherwise, in the case of very low values for the duty cycle (very narrow pulses), gate signals will be distorted.

Although EL7155 drivers are high performance 40MHz drivers, experimental results showed that for duty cycle lower than 10% (approximately 20ns for 5MHz of switching frequency), signal at the output of the driver is distorted (Figure 25), while the control signal at the output of the FPGA is without distortion. GaN HEMTs were able to work with this kind of distortion of the gate signals because of their lower threshold voltage, while the prototypes with Si MOSFETs needed higher driver supply voltage. In the case of GaN, voltage supplies for high-side and low-side driver were around 4.5V while for both Si prototypes were 5V.

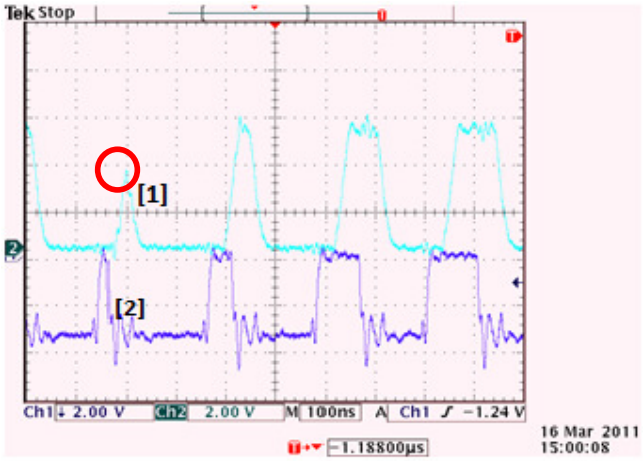

Figure 25: Distorted gate signal [1] and undistorted FPGA output signal [2]

After the statical efficiency measurements, 64QAM signal with 1MHz of bandwidth was generated. Applied input voltage was equal to 24V and switching frequency was set to 4.7MHz. In order to measure the efficiency in lower and higher power range (around 14W and 31W), output resistance was set to 15Ω and 6Ω, respectively. The obtained results are presented in Table 5 and 6. The measured efficiency included losses in both drivers and isolation chips.

The obtained results for average output power around 14W showed higher efficiency of a GaN prototype comparing to the both Si prototypes: 4.5% comparing with the prototype with BSC016N04LSG and 11.9% comparing with the one with BSZ097N04LSG. In the case of $P_{OUT,AVG}$ around 31W, Si prototype with BSC016N04LSG showed the highest efficiency, as it was expected from the efficiency curves presented in Figure 24.

	GaN	BSC016N04LSG	BSZ097N04LSG
$P_{out, avg}$[W]	14.4	14.2	13.8
Eff [%]	79.2	74.7	67.3

Table 5: Obtained results for 64QAM and R=15Ω

	GaN	BSC016N04LSG	BSZ097N04LSG
$P_{out, avg}$[W]	31.3	31.9	30.8
Eff [%]	85.9	92.2	75.3

Table 6: Obtained results for 64QAM and R=6Ω

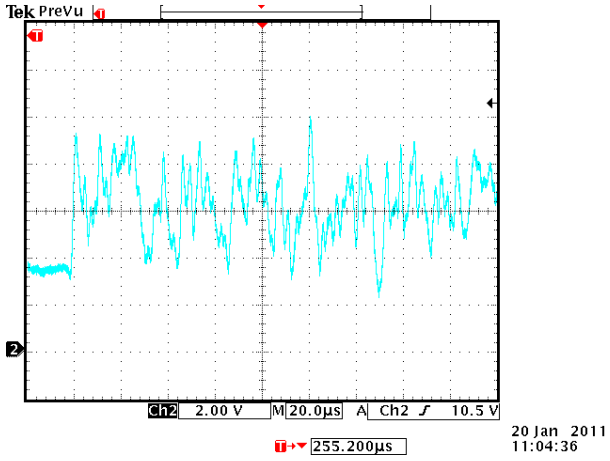

Figure 26: Generated 64QAM signal using the prototype with GaN HEMTs

After 64QAM, Wideband Code Division Multiple Access (WCDMA) sequence was generated and presented in Figure 27. With switching

frequency equal to 5MHz, input voltage of 24V and output resistance of 6Ω, envelope with the bandwidth of 500kHz was generated. Obtained results are presented in Table 7. Prototype with GaN showed 3% higher efficiency comparing to the prototype with BSC016N04LSG and 11.5% higher efficiency, comparing to the one with BSZ097N04LSG.

	GaN	**BSC016N04LSG**	**BSZ097N04LSG**
$P_{out,\ avg}$[W]	**16.3**	**16.1**	**15.8**
Eff [%]	**79.8**	**76.8**	**68.3**

Table 7: Obtained results for WCDMA signal with 500kHz of envelope bandwidth in the case of R=6Ω

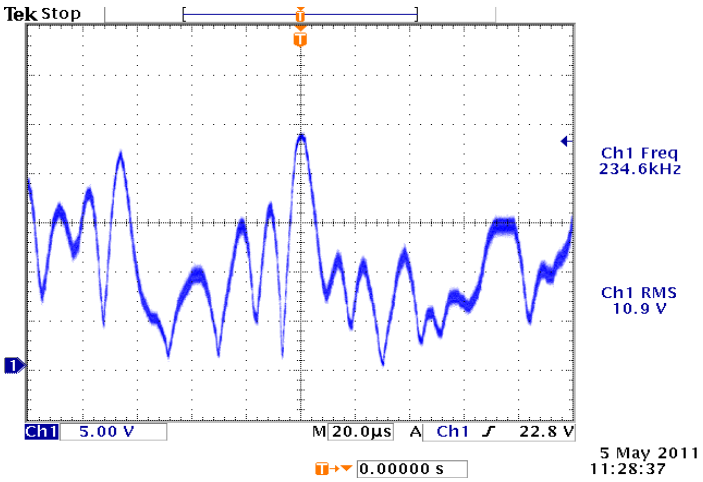

Figure 27: Generated WCDMA signal with GaN prototype

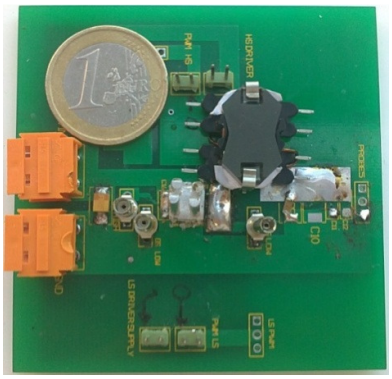

Figure 28: Prototype with GaN HEMTs

Chapter5. Conclusions and future work

I. Conclusions

Design of an Envelope Amplifier using new technological solution for switching devices based on Gallium Nitride and the filter design methodology for this application, were proposed in this thesis.
Filter design is very important issue in order to obtain the envelope with minimum possible distortion and on the other hand, to maximize the converter's efficiency by obtaining the optimum trade-off between conduction and switching losses. For a certain specifications regarding the input voltage, maximum output voltage swing, frequency of the generated sinusoidal waveform, desired attenuation of the filter and the output resistance, this filter design methodology determines the values for the inductor, capacitor and switching frequency for which, the optimum trade-off is obtained. This optimum efficiency point is strongly dependent on the load: for high load, the optimum point is shifted to the higher switching frequency, in order to minimize conduction losses which are dominant in the case of a high load and vice versa: for low load, optimum point is moved to the design which corresponds to the lower switching frequency in order to decrease the dominant switching losses.
The curve that represents power losses dependence on the filter design parameter A in the case of sinusoidal output voltage was derived and the efficiency optimum point was found, for several different loads. For one value of the load, the prototype with capacitor and inductor values determined in this way was made. Experimental results showed good correspondence with the model regarding the determination of the optimum efficiency point and verified the proposed methodology. The offset between the predicted and experimentaly obtained efficiency curve exists because the power losses model is not precise enough and needs to be improved.

To conclude:

- Filter design methodology provided the determination of optimum efficiency point, in the case of sinusoidal output voltage.

The second goal of this thesis was comparison of new power switches, GaN HEMTs with Si MOSFETs, in order to explore the benefits of WBG devices in the case of RF applications. In order to do this, three prototypes of synchronous buck were made: one with GaN HEMTs from EPC and two with Si MOSFETs with very good values for FOM. All prototypes were exactly the same, regarding the PCB layout and driving circuit. First of all, this comparison demanded determination of optimum operating conditions for each of three prototypes. When this was achieved, statical measurements were made, for different levels of the output power, achieved by the duty cycle change. This was performed because in the case of Envelope Amplifier, RF PA behaves as a constant resistive load while the duty cycle is being modified in order to generate the reference at the output. These measurements showed the highest efficiency of the prototype with GaN, up to 25W of the output power. Most likely, the efficiency of GaN prototype started to decrease because of the problems with power dissipation and the absence of the suitable package.

After statical characteristics, dynamical test with 64QAM and WCDMA signals were made. Comparing to Si MOSFETs, application of GaN HEMTs experimentally showed efficiency increasement of 5% for 64QAM signal with Pout approximately 14W and bandwidth of 1MHz, and increasement of 3% for WCDMA signal with Pout approximately 16W and bandwidth of 500kHz.

To conclude:

- GaN HEMTs showed better performance in a low power range which is important in the case of signals with high Peak-to-Average Ratio.

II. Future work

Regarding the future work, it is necessary to

- Develop a detailed model of power losses for GaN HEMTs.
- Implement drivers with a lower intrinsic delay in order to increase the switching frequency and bandwidth of the transmitted signals.

Speaking of filter design, it is necessary to

- Generalize the methodology for random signals such as WCDMA, in order to apply the proposed methodology in a real RF transmitter.
- Apply more detailed model for power switches in order to determine the optimum efficiency point more precisely.

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