Proyecto Fin de Máster

Design of envelope amplifier based on multiphase converter with Minimum time control

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Chapter1. Introduction

I. Objectives of the project

In the new power amplifier architectures which have both phase modulation and envelope modulation, the efficiency of power amplifier system depends on the drain efficiency and the efficiency of the envelope modulation circuit (envelope amplifier). Actually, the envelope amplifier can be described as a DC-DC converter with output voltage in proportion with envelope reference. Due to the demands of high efficiency and wide bandwidth in modern wireless communication system, the project in this thesis is to design an envelope amplifier pushing efficiency and bandwidth as high as possible with new solution we propose. However, the efficiency and bandwidth have inherent trade-off in the design that can be seen in the following sections.

II. Brief introduction of RF power amplifier

Nowadays the wireless communication is everywhere in our life, from cell phone to data transmissions in the space and the power range for the applications varies from several milliwatts to several kilowatts. The radio frequency power amplifier (RFPA) plays a crucial role in the wireless communication system, which has to amplify and reproduce the electric signals in order to transmit them. There are two main characteristics that usually are used to categorize the classes of RFPA, linearity and efficiency. Different classes of RF power amplifiers have different linearity and efficiency characteristics, which is defined by class A, B, C, D, E etc. but a class of RFPA with high efficiency is usually the one that has very poor linearity. The trade-off between the linearity and the efficiency always exists in RFPA.

Some signal modulations like Frequency Modulation (FM) or Frequency Shift Keying (FSK) with constant envelope do not need a linear amplifier and therefore high linearity is not necessary. But high linearity is very important when the techniques include both amplitude and phase modulation of the input signal, such as Quadrature Phase Shift Keying (QPSK) and Quadrature Amplitude Modulation (QAM) which use amplitude modulated signals. Distortion of the amplified signal can be caused by two kinds of

nonlinearities: amplitude nonlinearity and amplitude to phase distortion. The amplitude nonlinearity is related to the saturated transistors inside the used PA or variable gain of the amplifier. This distortion can be observed by comparing output signal envelope with the reference received by PA. The amplitude to phase distortion is related to the voltage-variable capacitances in the devices [1]. It can be described as phase shift between amplitude and phase of output signal. Both nonlinearities can be measured by changing the input signal amplitude slowly and measuring the output signal amplitude and phase related to the input signal, and can be mathematically described as follows:

$$(A_m(t) + f_{AM-AM}(V_{In}(t))\cos(2\pi f_c + \phi(t) + \theta_{AM-PM}(V_{In}(t))) \quad (1)$$

Where $A_m(t)$ is the desired amplitude modulation, f_c is the carrier frequency, $\Phi(t)$ is the desired phase modulation, and $f_{Am\text{-}Am}$ and $\Theta_{AM\text{-}AM}$ are amplitude distortion and amplitude to phase distortion. Additionally, there are also other well-known nonlinearities resulting from thermal effects or charge storage [2].

There are different techniques for measuring and characterizing the linearity of RFPAs, depending on the signals in applications. One of the most traditional techniques is based on carrier to inter-modulation ratio (C/I). The RFPA is driven with two-tone carrier (two carrier signal with close frequencies) of equal amplitudes. Nonlinearity of the RFRA introduces inter-modulation distortion (IMD) products in the spectrum of the RFPA output, which are close to the carrier frequency. The third order or the maximal IMD is compared with the amplitude of the carrier to obtain the C/I ratio.

Noise-Power Ratio (NPR) is another method that can be used to measure the linearity of PAs for broadband. In the communication system, the noise includes Inter-modulation Noise, Atmospheric Noise and Thermal Noise. Inter-modulation Noise is caused by nonlinearities in a receiver or transmitter. The PA is driven with Gaussian white noise in order to simulate the presence of many carriers of random amplitudes and phases. The white noise is first passed through a band-pass filter and then through a filter with a notch in one segment of its spectrum. The amplification produces IMD products, which cause power to appear in the notch. The power of the output signal is observed in the notch and NPR is calculated as the ratio of the notch power to the total signal power [3].

Adjacent Channel Power Ratio (ACPR) characterizes how the nonlinearity affects adjacent channels and is widely used with modern shaped-pulse digital signals such as CDMA. ACPR represents the ratio between the total power of the adjacent channel (signal produced by the amplifiers nonlinearities) and the power of the main channel (useful power) [3].

Error Vector Magnitude (EVM) is a convenient measure of how nonlinearities interfere with the detection process. EVM is defined as the distance between the desired and actual signal vectors, normalized to a fraction of the signal amplitude.

The nonlinearities are common in RFPA, therefore the linearization is needed when both amplitude and modulation are required. There are several techniques that can be used for linearization of RFPA. The feed-forward amplifier linearization technique is used to remove both inter-modulation distortions and linear distortion. Linear distortion is a term used when there is non-ideality in the gain and phase response. Pre-distortion techniques have been widely used for linearization of RF power amplifiers. The response of pre-distorter is constructed based on the AM-AM and AM-PM distortion of the power amplifier [4-5]. Modeling of the PA nonlinear behavior allows correction for not only the AM-AM and AM-PM distortion but also for other nonlinearity effects. Adaptive pre-distortion is also introduced to correct for the pre-distorter coefficients using a feedback loop.

To improve the efficiency as high as possible is the other goal in RF power amplifier or the systems including RFPAs design. There is an inherent relation between linearity and the efficiency of a RFPA, as mentioned before. In general, the more linear a RFPA Is, the lower its efficiency will be. In the wireless system, the RFPA is one of the most power consuming devices. Therefore improving the efficiency of the RFPA is very critical. The RFPA efficiency can be defined as:

$$\eta = P_{out}/(P_D + P_{DC}) \tag{2}$$

P_D is the power consuming in the supporting circuits, and P_{DC} is the DC power. In the definition of efficiency, instantaneous efficiency is the efficiency at one specific output power. For most of the RF power amplifiers, the instantaneous efficiency varies with output power. The highest efficiency is obtained at the peak value of the output power and decreases as the output power decreases. When the signal includes amplitude modulation, the output power changes in time and, as a result, the instantaneous efficiency of

the RFPA changes in time. For this situation, a good efficiency measurement is the average efficiency method, which is the ratio of average output power to the average DC input power [1]. This efficiency can be estimated by using amplitude density distribution of the amplified signal.

III. Efficiency problem of non-constant envelope modulations

The number of wireless subscribers grows tremendously in recent years. Moreover, new services like music downloads, video call and Internet access on wireless cell phones have meant more and more data transmissions over wireless infrastructures. At the same time, however, the frequency spectrum allocated for wireless communications has been essentially constant. But with more users and more traffic, the wireless spectrum has become very crowded. To solve this problem, wireless providers have switched to wireless standards that use the spectrum more efficiently. The wireless standards CDMA2000, W-CDMA, TD-SCDMA, MC-GSM, WiMAX and LTE were all deployed or defined to improve spectral efficiency. Figure 1 shows the wireless standards deployed or defined in recent years to improve spectral efficiency [6].

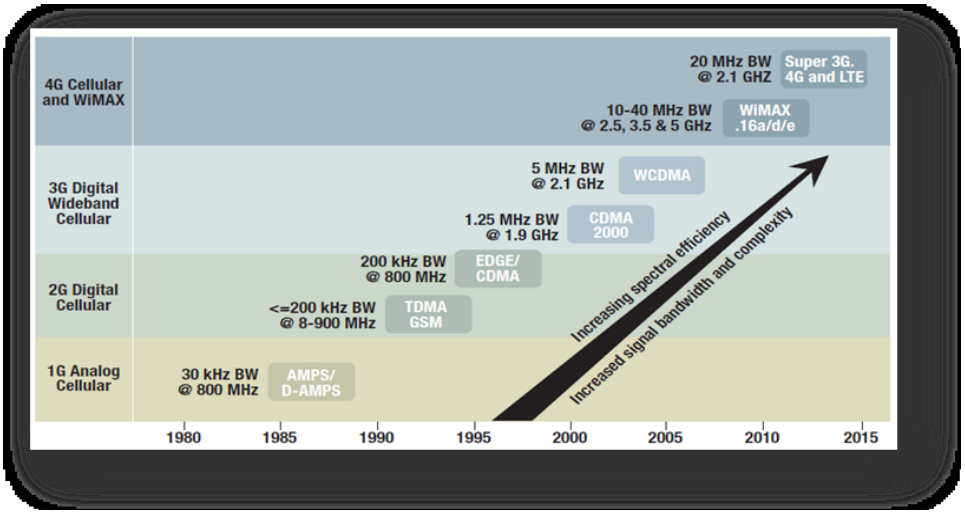

Figure 1: Evolution of wireless standards.

Nevertheless, the new wireless standards use complex modulations based on multicarrier signals. These modulations employ both envelope and phase

modulation and result in complex non-constant envelope. Due to such a complex signal, high linearity is necessary. Unfortunately, traditional linear PAs such as class A, B or AB have low efficiency. For example, a class B amplifier has efficiency of π/4, but only in the case when it amplifies a sine wave of the maximal amplitude. Figure 2 shows the efficiency of class A and class B amplifiers depending on the amplitude of the amplified sine wave. However, the signals in new wireless standards have a very high peak-to-average ratio (PAR), for example WCDMA's PAR is between 9dB and 11dB. In order to obtain high linearity, the linear RFPA using back-off technique is supplied by voltage higher than the maximal signal amplitude [7]. This leads to a lot of power losses. Even more, if the most part of the signal distribution is below the average value, the efficiency will be quite low. The signal probability distribution in new wireless standards is also shown in Figure 2, which is usually presented as Ralyeigh's distribution. It can be seen that the signal probability density is very high in the zone where the linear PAs have low efficiency.

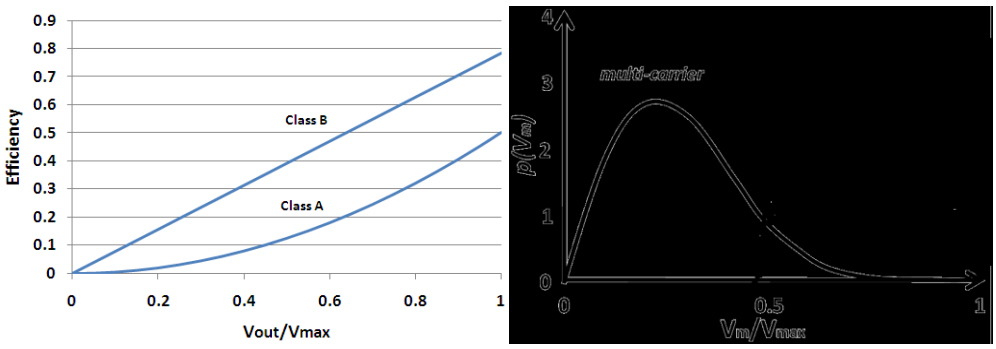

Figure 2: Efficiency of class A and class B amplifiers for different values of amplitude of the amplified sine wave(left) and the wireless envelope probability distributions (right)

IV. High efficiency techniques for RFPA

With the growing emphasis on channel capacity, the new generation of the communication systems use non-constant envelope RF signals to increase capacity. Unfortunately, the amplification of non-constant envelope signals

requires linear power amplifiers, which inherently have low efficiency. As explained above, the traditional approach that uses linear amplifiers to modulate amplitude has poor efficiency. There are two techniques that have been proposed in order to improve the efficiency of PAs for non-constant envelope amplification, envelope elimination and restoration (EER) and (envelope tracking) ET.

Envelope Elimination and Restoration-EER

This technique was proposed by Kahn [8]. It combines highly efficient switching mode RFPA (like class E or class F) with a high efficiency envelope modulation circuit in order to obtain linear RFPA with high efficiency. The idea is based on the principle that any narrow-band signal can be represented as simultaneous envelope and phase modulations. The mathematical representation can be:

$$V_{RF}(t) = I(t)\cos(2\pi ft) - Q(t)\sin(2\pi ft) = A(t)\cos(2\pi ft + \theta(t)) \tag{3}$$

$$\theta(t) = arctg(\tfrac{Q(t)}{I(t)}), A(t) = \sqrt{I(t)^2 + Q(t)^2} \tag{4}$$

where f is the carrier frequency, Q(t) and I(t) are the modulated signals. In Figure 3 a simplified block schematic of Kahn's technique transmitter is shown and there can be distinguished two main parts: the first part serves for the implementation of the envelope modulation done through the envelope amplifier, while the second one is used for phase modulation.

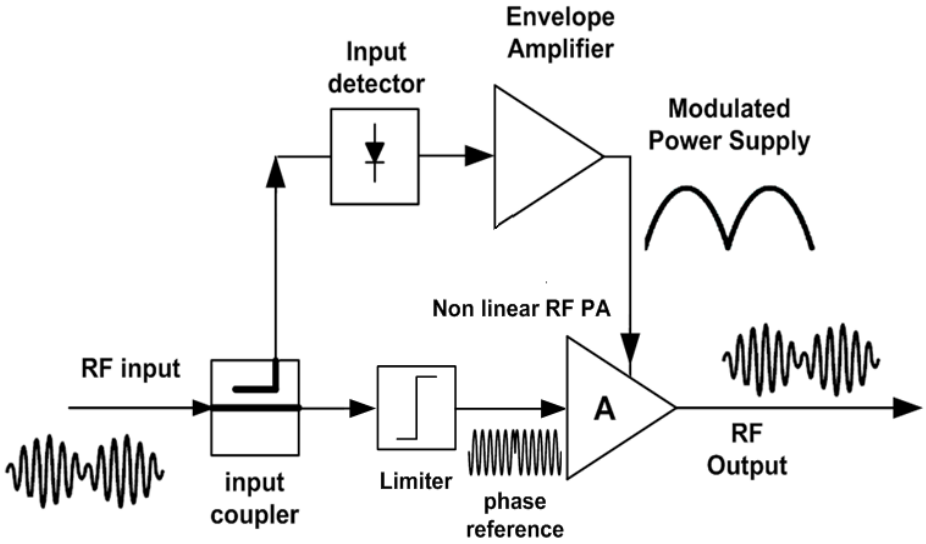

Figure 3: Block schematic of a transmitter based on EER technique

As it can be seen, the total efficiency of the transmitter based on the Kahn's technique is, approximately, the efficiency of the envelope amplifier multiplied by the efficiency of the nonlinear RF PA. The nonlinear RFPA such as Class E usually have efficiency over than 90%. If high efficiency of the envelope amplifier can be obtained, Kahn-technique transmitter can achieve high efficiency.

The linearity of the transmitters based upon the EER technique depends upon the modulator rather than the RF-power transistor and this leads to very high linearity of the system. The two most important factors that influence the linearity in this technique are the bandwidth of the envelope amplifier and the time alignment of the envelope and phase modulation. The analysis done in [8] shows that the envelope bandwidth must be at least twice the RF bandwidth and the misalignment between the two modulations should not exceed one tenth of the inverse of the RF bandwidth. Regarding the envelope amplifier, there are several properties that must be satisfied, such as:

- High linearity
- High efficiency
- Very fast dynamic response

- Minimal interference with the spectrum of the transmitter's output signal

There are numerous state of the art solutions that are mostly based on employing dc-dc converters, and a short summary of these solutions will be presented in the next chapter. In this summary, each solution will be evaluated according to the before mentioned properties that it must fulfill.

Envelope Tracking-ET

This technique is quite similar to the EER technique. The supply voltage of the transmitter is varied dynamically, according to the signal's envelope, but with certain excess in order to allow the RFPA to operate in a linear mode. The envelope and phase modulation are done through the linear RF PA, and the supply voltage is varied just to save the energy. Therefore, the linearity of such a like transmitter is completely dependent on the employed RFPA. Figure 4 shows the block schematic of envelope tracking technique.

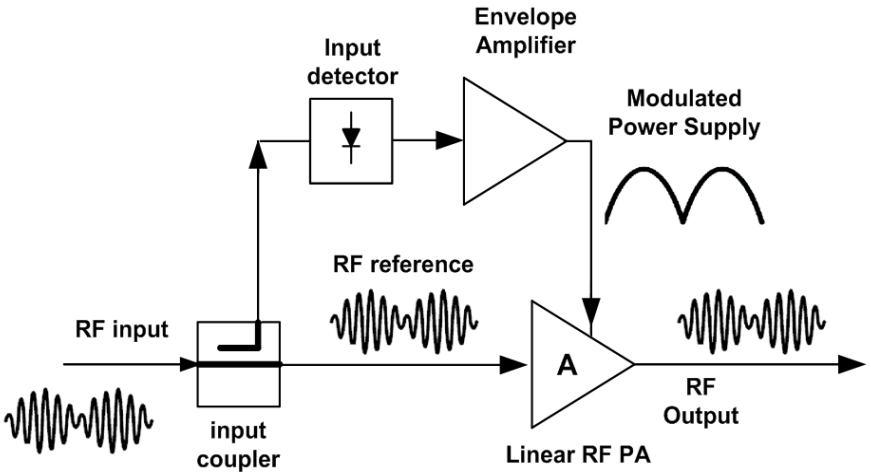

Figure 4: Block schematic based on envelope tracking

As in the case of the Kahn's technique, the solutions for the power supply that can vary its output voltage are similar, but the main difference is that the power supply for envelope tracking is not as crucial as in EER technique and its tracking precision and speed do not need to be so precise and high as in EER. If the RF PA is implemented as a class A amplifier, its bias current can also be varied.

The efficiency of the transmitter that uses this technique is significantly better than in the case of a linear RF PA that is supplied from a constant power supply, but, nevertheless, still lower than theoretical efficiency of the EER technique transmitter. Figure 13 presents the instantaneous efficiency of the RFPA depending on which technique is used (EER, ET or constant supply). In the case of a class B amplifier and a linear amplifier that employs ET, it is assumed that the minimal voltage drop on the power transistor is 15% of the maximal supply voltage. The efficiency of a transmitter that uses EER technique is estimated as the product of the efficiencies of a class E amplifier and a switching converter that acts as the envelope amplifier. Its efficiency can be flat for a wide range of output power.

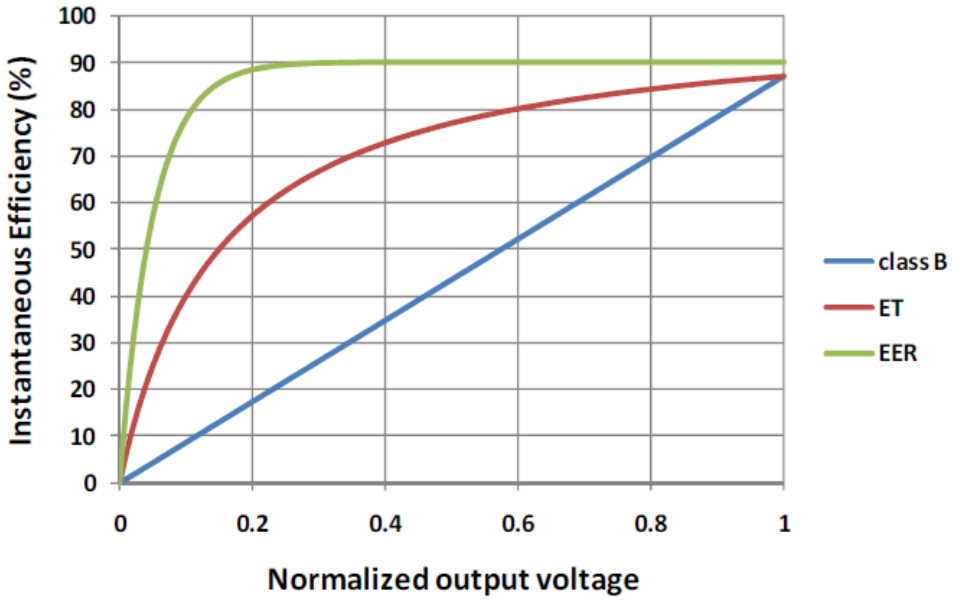

Figure 5: Instantaneous efficiency of RFPA with different techniques

Chapter2. Envelope amplifier

As it has been aforementioned, the envelope amplifier should have fast dynamic response, high efficiency and minimal interference with the output spectrum of the transmitter. Having these specifications in mind there can be found several solutions in the state of the art depending on the simplicity, bandwidth and efficiency of the envelope amplifier.

I. Linear regulator

Linear regulator is the simplest one, and it is applied when the main concern is to provide a simple voltage supply modulation and low cost solution. Usually, when a linear regulator is applied, the efficiency of the envelope amplifier is not of primary concern. The main idea is to use a transistor as a voltage controlled voltage drop in order to control the output voltage, as it is shown in Figure 6.

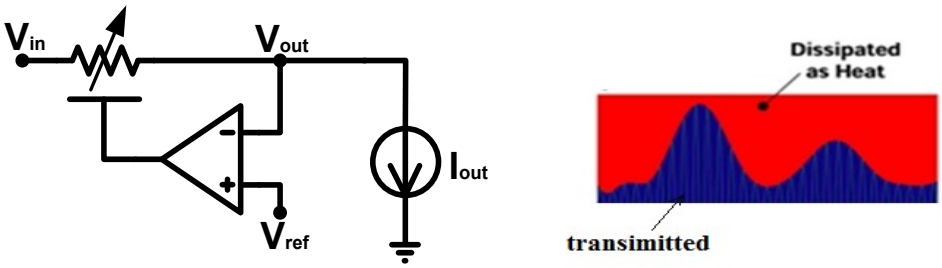

Figure 6: linear regulator

Unfortunately, its main disadvantage is the low efficiency, because its ideal instantaneous efficiency is equal to:

$$\eta = \frac{V_{out}}{V_{DD}} \tag{5}$$

However, with this solution it is possible to achieve high bandwidth and high linearity of the envelope amplifier. Due to the high linearity of the linear regulator, the interference with the output spectrum of the transmitter is low

and, additionally, it filters high frequency noise that can enter through the voltage supply. Due to its simplicity, fast linear regulator with small die areas can be easily integrated. In [9] a 1 A linear regulator in 90 nm CMOS technology and over 100 MHz bandwidth is reported. In [10] a linear regulator is implemented as the solution for the envelope amplifier and integrated with the rest of the RF transmitter. In both applications, the necessary bandwidth of the envelope amplifier is in the MHz range and the output power is very low, between 0.5 W and 2.2W. In the case of [10] it is said that the linear regulator is supplied by 3.3 V and that the average value of the envelope is 1.9 V. Based on this information, the average efficiency of the envelope amplifier for the applied EDGE modulation can be estimated at 57.5%.

II. Switching DC-DC converter

To achieve high efficiency it is necessary to use a voltage regulator based on switching dc-dc converter. These regulators use transistors as switches in order to convert the input voltage to different voltage levels. By controlling the fraction of time when the switch is turned on (duty cycle) it is possible to change the level of the output voltage. The two most used topologies are the buck and the boost converters, which decrease and increase the input voltage, respectively. In the applications when it is necessary to be able to increase and decrease voltages with only one converter it is possible to use a buck-boost converter. Figure 7 shows the waveform of envelope tracking with buck converter.

Whatever topology is selected, there are always two parts that always can be distinguished. The first is the switching network and the second is the low-pass output filter. The bandwidth of the converter, the ripple of the output voltage and the converter's efficiency depend on the selection of the switching frequency and the design of the low pass filter. Unfortunately, some of the requirements are contradictory. For example in order to achieve high bandwidth it is necessary to apply high switching frequency and it leads to high switching losses, decreasing the converter's efficiency. Another possibility would be to move its corner frequency to higher frequencies, but it would lead to high voltage and current ripple. Therefore, if a switching converter is optimized for the envelope amplifier it is necessary to design it

applying a trade-off in the way that it has sufficient bandwidth and high average efficiency. Normally, the bandwidth of the switching converter can be estimated as one fifth of the switching frequency in the case of a buck converter. If a boost or buck-boost converters are used the bandwidth is even less, due to the right half plane zero that is present in these topologies.

Another important issue is the additional spectral components that are introduced by the switching converter. By modulating the value of the duty cycle it is possible to reproduce the desired envelope, but the spectral content of the converter output voltage has additional spectral component around the converter's switching frequency and its multiples.

When the converter has been designed, it is good to know the converter's closed loop frequency characteristics. In Figure 8 a typical Bode plot of the transfer function (from the duty cycle to the output voltage) of a buck converter is shown. The block diagram of a switching converter with closed control loop is shown in Figure 9. By good design of the compensator it is possible to achieve a bandwidth of the system higher than the corner frequency of the converter, but only for small signals. In the case of the envelope amplifier the duty cycle has to be able to make excursions from its minimum (zero) to its maximum (one). If the reference frequency is higher than the corner frequency, at the output of the compensator the desired signal is higher than one, in order to compensate the attenuation of the converter's characteristics. However, the duty cycle cannot be higher than one, and the output signal of the compensator will be saturated to this value. In this way, we can see that the bandwidth of the envelope amplifier implemented by a switching converter is limited by the corner frequency of the converter.

As a consequence, the corner frequency of the open loop frequency response should be higher than the maximal spectral component in the transmitted envelope in order to guarantee that all the spectral components of the envelope will be reproduced with the same gain. Beyond the corner frequency the gain of the converter starts to fall and, therefore, the corner frequency of the converter can be considered as the bandwidth of the converter. The switching frequency should be much higher than the corner frequency in order to suppress all the additional harmonics in the spectrum that are present due to the switching.

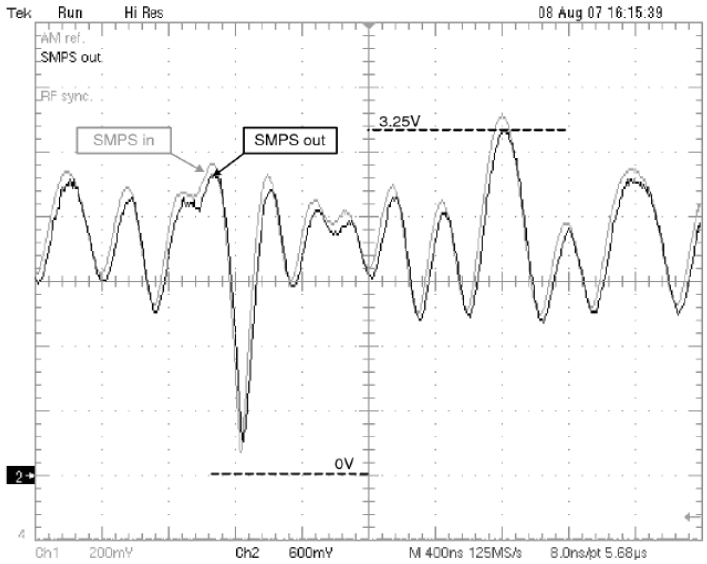

Figure 7: waveform of envelope tracking with switching DC-DC converter

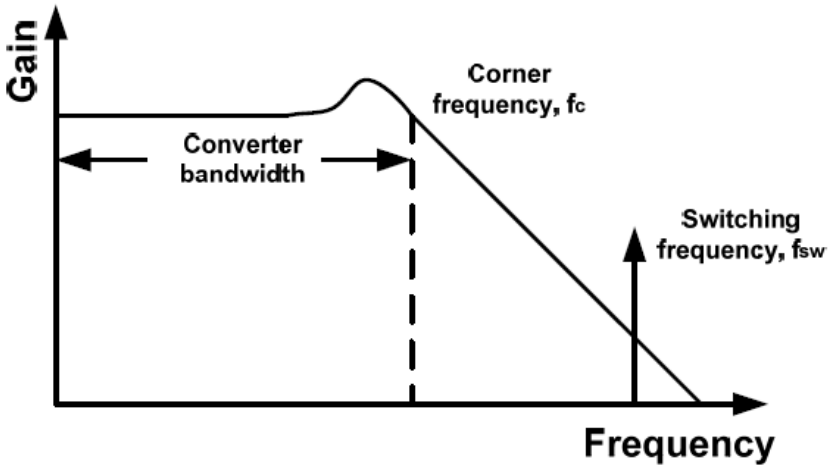

Figure 8: typical frequency response of a switching converter

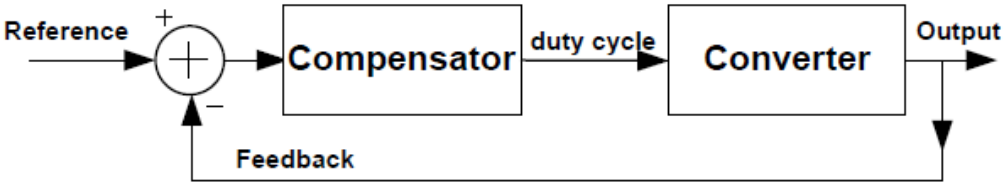

Figure 9: block diagram of switching converter with close control loop

The low pass filter is usually designed as a simple two-pole LC filter. However, in [11], a double LC filter is proposed in order to enhance the attenuation of the additional spectral components and to decrease the voltage ripple of the output voltage. In [12] it is shown that more complicated filters can be used in order to satisfy the levels of attenuation of the output filter and that the switching frequency necessary to apply the switching frequency has to be at least 5 times higher than the bandwidth of the reproduced envelope. In [13] the switching frequency is even 20 times higher than the bandwidth of the envelope. A switching frequency of 3.3 MHz is used in order to reproduce a 150 kHz sine wave.

In the state of the art there can be found many examples where a simple buck converter can be used as the envelope amplifier. The envelope bandwidth differs a lot, from 12 kHz up to 20 MHz [14], and in that way the switching frequency as well from 200 kHz to 130 MHz [14]. The output power varies as well. The output power of these envelope amplifiers goes form tens of milliwatts up to several hundreds of watts [11].

Solutions that employ high switching frequencies are normally integrated, because it is demonstrated that parasitic elements, especially parasitic inductances in the MOSFET terminals, have huge impact on converter's overall efficiency. By integrating the converter, these parasitic inductances are significantly reduced, and it is possible to use high switching frequencies. One problem of this approach is that the output power of the converter is usually low, due to the size of the implemented MOSFETs and the maximal current they can withstand. Therefore, one common property for all the solutions is that high bandwidth/high switching frequency prototypes are used for low power applications.

A simplified schematic of one possible EER PA, where the envelope amplifier is made as a buck converter and non-linear amplifier is a class E amplifier, is shown in Figure 10.

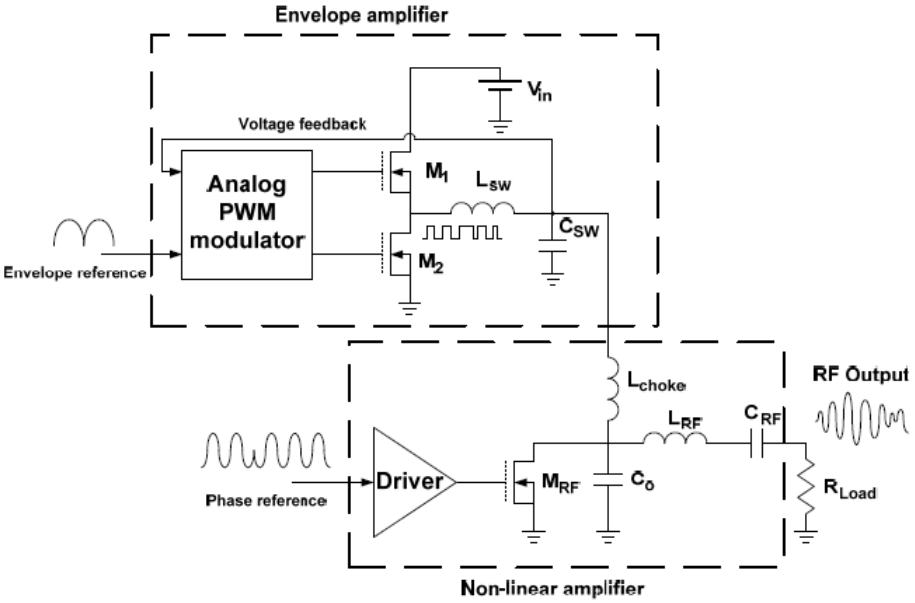

Figure 10: PA base don EER technique

In [15] a multiple input buck converter is presented as one possible solution for the envelope amplifier. The implemented envelope amplifier can provide up to 100W and reproduce 100 kHz sine wave.

In order to maximize overall efficiency and minimize ripple of the output voltage several converters can be interleaved like it is shown in Figure 11. Interleaving can lead to higher overall efficiency and small voltage ripple [16]. By interleaving several buck converters and governing them in a time shifted way it is possible to achieve ripple cancelation and, in that way, reduce the inductance and capacitance of the output filter which, additionally, leads to good dynamic properties of the converter. In [17] an envelope amplifier implemented by interleaving four buck converters was presented. The presented enveloper amplifier can provide up to 240 W of instantaneous power with efficiency of 95%, while the bandwidth is around 30 kHz. One of the disadvantages of this technique is the possibility of unbalanced current sharing among the phases and that the control becomes more complex with higher number of phases. Although the dynamic of the interleaved converters is better than the dynamic of the single one, the bandwidth of interleaved converters does not increase linearly with the number of applied levels [18], and for wide bandwidth envelopes it is still necessary to apply high switching frequency.

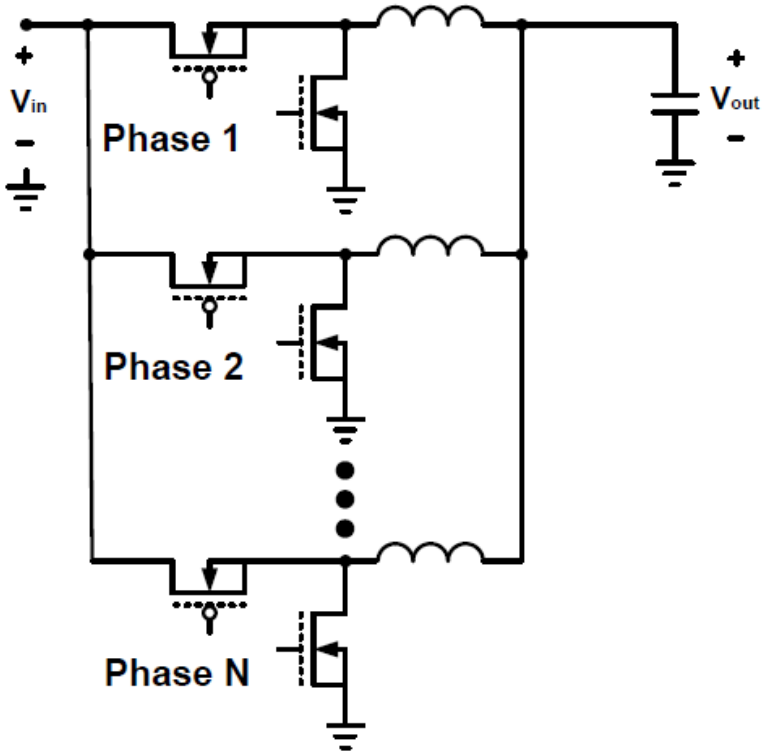

Figure 11: Schematic of multiphase buck converter

III. Switching DC-DC converter in parallel with linear

In order to combine the good bandwidth characteristics of linear regulator and the high efficiency of switching converters a solution based on parallelized linear regulator with a switching converter is sometimes employed. In this way, the slow dynamics that suffer switching converters is compensated by the parallel linear regulator. A simplified schematic is shown in Figure 12. The main role of the linear regulator is just to give sufficient current in order to avoid distortion of the output signal, while most of the energy is processed through the switching converter. Some examples of this solution can be found in [19]. The idea is that each part of the envelope amplifier should reproduce certain part of the envelope's spectrum. By analyzing the spectrum of the envelope signal, it can be concluded that the major part of the envelope's energy lies in the region of low frequency components that can be easily and efficiently reproduced by a switching power converter. The non-efficient linear regulator does not have to handle a

big portion of the envelope's energy, and its task is just to reproduce the part of the spectrum that is necessary in order to obtain the correct envelope. If the transmitted signal is known, it can be found an optimal frequency for band separation where the efficiency of the envelope amplifier is maximal. In this way, it is possible to obtain high linearity, high efficiency and high bandwidth, but one of the problems is the separation of the spectrum. The envelope reference has to be separated in two references, as it is shown in Figure 12, through the low-pass and the high-pass filters, and later, when the linear regulator and switching converter reproduce their references, these voltages have to be summed. The processes of band separation and summation must be done correctly in order to maintain high level properties of the envelope amplifier implemented in this way.

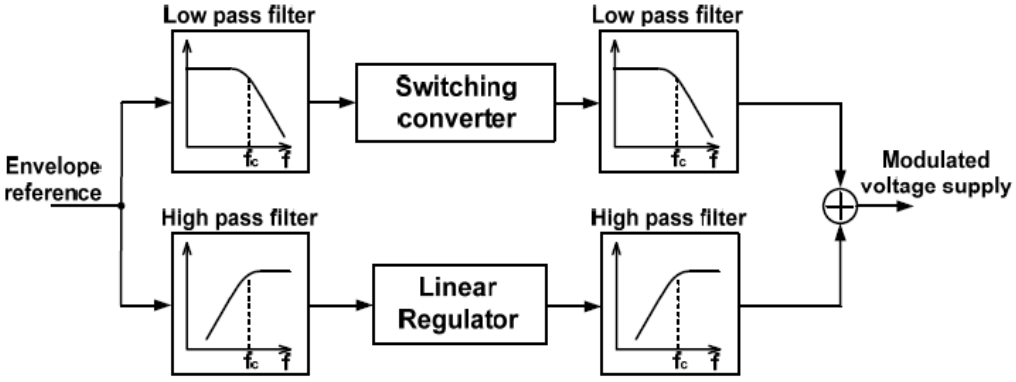

Figure 12: Envelope amplifier using a switching converter in parallel with linear regulator

A simplified schematic of an envelope amplifier implemented using a buck converter in parallel with a linear regulator is shown in Figure 13.

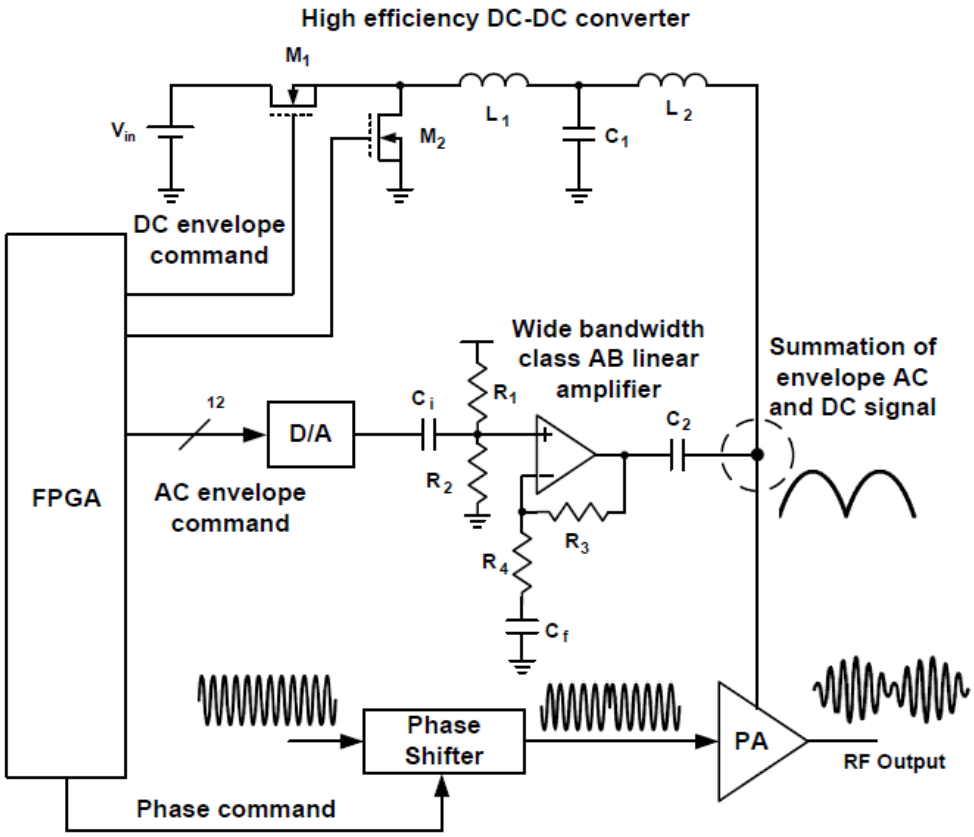

Figure 13: envelope amplifier implemented using a buck converter in parallel with a linear regulator

IV. Multilevel converter in series with linear regulator

The linear regulator, as an envelope amplifier explained above, can provide wide bandwidth, wide output range, and high linearity, but the limitation is low efficiency, especially when the envelope has high PAR. In order to improve the efficiency of the linear regulator, it can be supplied by a modulated voltage, which is modulated in the same way as the envelope of the transmitted signal.

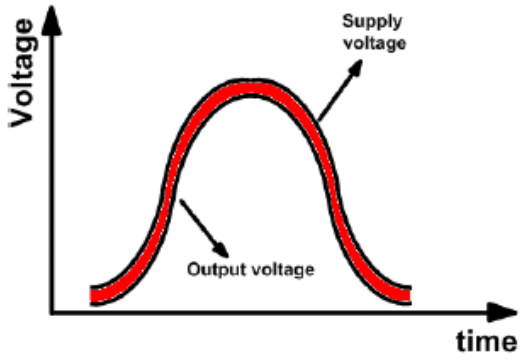

Figure 14: Supply and output voltage of linear regulator in the proposed solution of envelope amplifier

As long as the modulated supply voltage is higher than the expected output voltage, the linear regulator operates correctly. Naturally, depending on the transistor that is used as the regulator's pass element, the minimal difference between supply and output voltage will vary. In the case of an ideal linear regulator, the minimal voltage difference is assumed to be zero volts. The losses of the linear regulator depend on the voltage drop on the employed pass element and the load current, and can be calculated as follows:

$$P_{losses} = (V_{supply} - V_{load}) I_{load} \tag{6}$$

Depending on the type of load, whether it is a current source or a resistance, the losses of the linear regulator will differ. Figure 14 shows how the power losses of a linear regulator depend on the output voltage in the case when it is supplied by a constant and by a modulated voltage and the load is a current source. In the case of the modulated voltage supply, it is assumed that the voltage difference between the output voltage and supply voltage is constant.

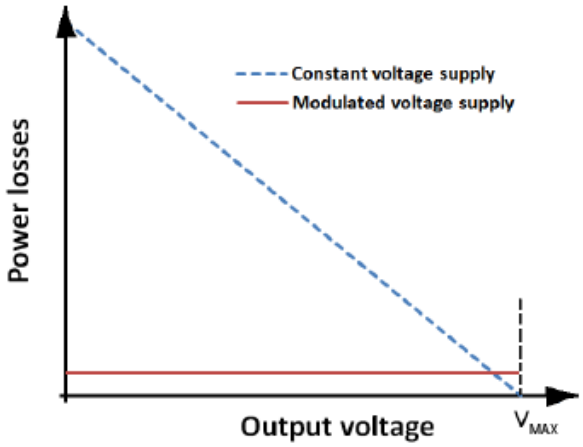

Figure 15: Dependency of the power losses in linear regulator on its output voltage with current source load

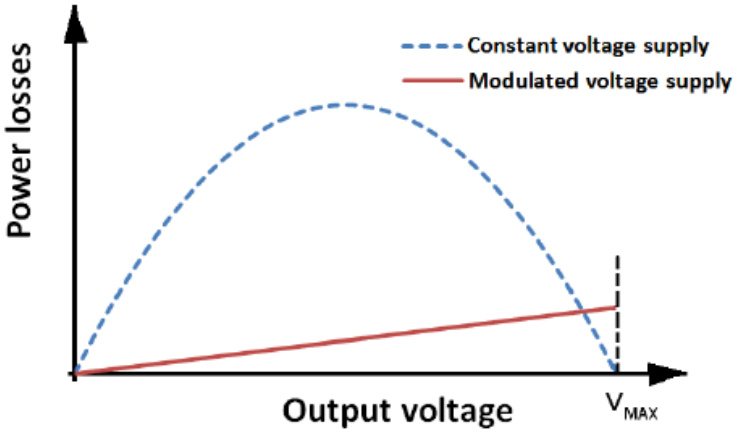

Figure 16: Dependency of the power losses in linear regulator on its output voltaje with resistance load

If the load is a resistance, the power losses depend on the output voltage as it is presented in Figure 16. For both types of loads, average power losses of the linear regulator can be significantly decreased by using the modulated voltage supply for the linear regulator. In any further consideration of the load for the envelope amplifier, it will be assumed that it is purely resistive, because the non-linear class E amplifier used as the actual load of the envelope amplifier behaves as a resistance.

By modulating the power supply of the linear regulator its efficiency is increased. However, in order to obtain high overall efficiency of the envelope

amplifier it is necessary to modulate the power supply by using a high efficiency, dc-dc switching converter. And both stages should receive the same reference signal, but the output voltage feedback should be applied only for the linear regulator. The dc-dc switching converter will operate in open loop and the tight regulation of the output voltage will be done by the linear regulator. The main role of the switching converter is to provide the supply voltage to the linear regulator, which, in other hand, has to manage all the regulation of the output voltage. The supply voltage of the linear regulator has to be always higher than the expected output voltage in order to guarantee the correct work of the linear regulator but, at the same time, the difference between these two voltages should be as close as possible in order to minimize the power losses of the linear regulator. Therefore, it can be said that the efficiency of the complete system will depend only on the efficiency and precision of the dc-dc converter.

By using the architecture proposed in this thesis, it is possible to take advantage of all the good characteristics of the linear regulator (high bandwidth, high linearity, etc.) and to obtain significantly higher efficiency comparing it with the solution when the linear regulator is supplied by a constant voltage. Additionally, the need for the complicated output filter design is avoided because most of the switching noise that comes from the switching converter will be filtered by the linear regulator and the feedback loop that is used can be very simple.

Thanks to the linear regulator that is employed as a post regulator, the output voltage will not have any voltage ripple, which is always present if only a switching dc-dc converter is used. In some applications for the envelope amplifier, the specifications for the voltage ripple, and not the desired bandwidth, lead to the necessity of very high switching frequency [11]. The main disadvantage of this architecture is that it is composed of two stages, and in order to obtain high efficiency of the envelope amplifier, it is necessary that the efficiency of both stages should be as high as possible. The efficiency of the linear amplifier will depend on the regulating precision of the dc-dc switching converter, and in order to obtain good precision for the linear regulator's input voltage the switching converter should operate at the switching frequency that is at least 5 times higher than the desired bandwidth of the envelope amplifier's output voltage [12]. If the requested bandwidth is 2 MHz, the switching frequency should be 10 MHz. At such a high switching frequency the efficiency of conventional converters (buck, boost, buck-boost etc) drops heavily due to high switching losses.

In order to decrease the switching losses in the converter that supplies the linear regulator another approach must be made. The linear regulator's input voltage does not have to be exactly its output voltage plus desired voltage drop. Its input voltage could be a rough approximation of the desired output voltage. This approximated voltage will not influence on the operation of the linear regulator as long as it is higher than the desired output voltage.

The easiest way to approximate the input voltage is to discretize it. This could be done easily by employing a multilevel converter as the power supply for the linear regulator. The proposed topology, a multilevel converter in series with a linear regulator, as a solution for the envelope amplifier is one of the original contributions of this thesis. Figure 17 presents time waveforms of the envelope amplifier that consists of a multilevel converter in series with a linear regulator.

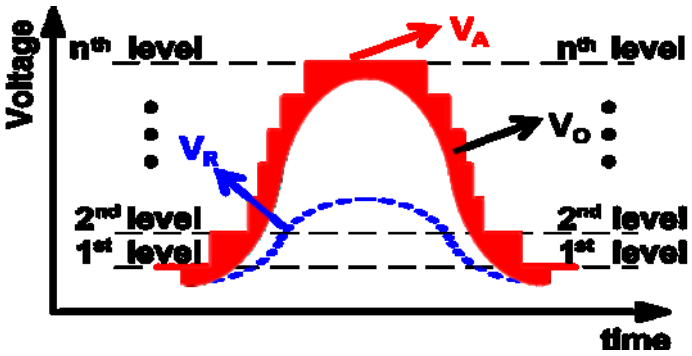

Figure 17: Time diagrams of multilevel converter solution for envelope amplifier

Chapter3. The proposed solution

I. Solutions for multilevel converter

Multilevel converters are usually employed as a solution for inverters. It can generate a sine wave applying discrete voltage levels. Some loads, like the electric motors for examples, behave as a low pass filter and, therefore, the staircase approximation of the sine wave is filtered by the load itself. On the other hand, sometimes it is necessary to design a low pass filter and introduce it between the multilevel converter and the load. The majority of the multilevel solutions are based on flying capacitors and in the fact that the reproduced signal is always a sine wave [20]. In the case that the signal to be synthesized is defined by its probability distribution, the time that the signal spends in certain level interval cannot be distinguished exactly, as in the case of a sine wave. These time intervals are easy to determine for deterministic signals (like a sine wave). However, two nondeterministic signals with same probability density can have different time behavior and it is difficult to estimate the time intervals the signal spends at each level. This is very important because in most of the solutions based on flying capacitors these capacitors are approximately equally charged and discharged during one period of a sine wave, and, in that way, the voltage levels that are used are roughly equal. In the case of a nondeterministic signal this equilibrium cannot be guaranteed. A 5-level multilevel converter based on flying capacitors is shown in Figure 18.

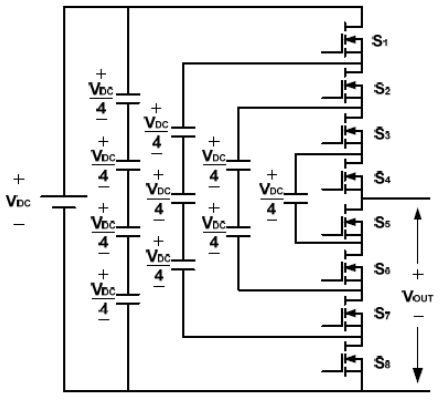

Figure 18:Simplified schematic of multilevel converter based on flying capacitors

In order to balance the capacitor charge and discharge it is necessary to use two switch combinations in one or several fundamental cycles. Nevertheless, if the period of the signal is not known, it is very complicated to apply a correct combination of switches in order to maintain the desired voltage levels. A similar problem can be noticed when this type of converter is used as an inverter and the load is reactive, not only resistive.

Therefore, two multilevel solutions in the envelope amplifier have been proposed based on other methods. One of the solutions is based on independent voltage cells. There are two stages in this solution, and first one is a single input multiple output converter. The second stage is composed of independent voltage cells that are put in series. The output voltage is obtained by the combination of cells' voltage, as shown in Figure 19. These cells can be implemented to give just positive and zero voltage (two-level cell), or to produce positive, negative and zero voltage (three-level cell). When the cell is turned on it provides a constant voltage, and when it is turned off it gives zero.

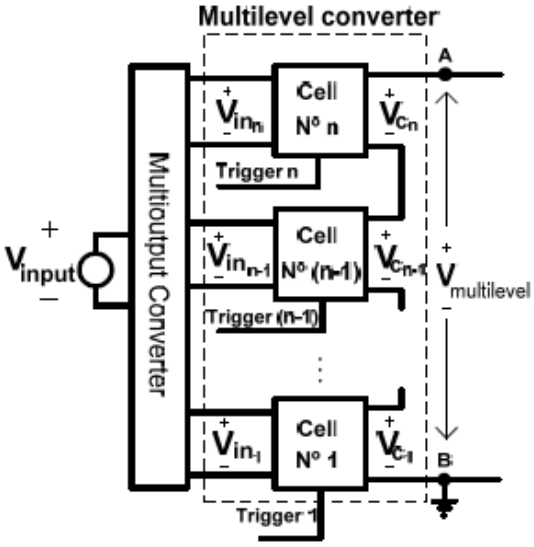

Figure 19: block schematic of multilevel converter based on independent voltage cells

The other solution is based no independent voltage sources [21]. The independent voltages are connected to the analog multiplexer that selects the voltage source depending on the level of the reference signal. The idea of this solution is shown in Figure 20. It is easy to see that in the case of the multilevel converter with N levels it is needed to have N voltage sources and

to employ N-1 MOSFETS and N-1 diodes. When a branch in the multiplexer conducts, there are conduction losses due to the resistance of the used MOSFET and voltage drop on the diode.

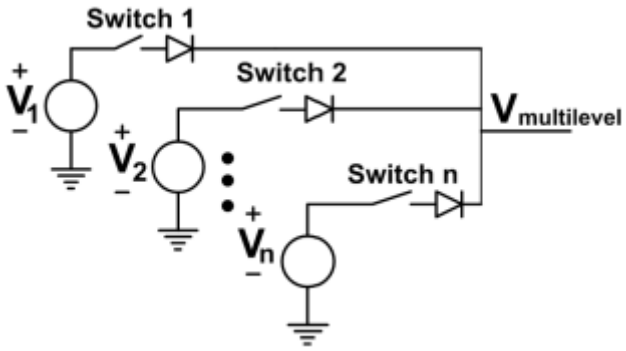

Figure 20: multilevel converter based on independent supplies and analog mutiplexer

II. The proposed multilevel converter

The problem of the solutions mentioned above is that the circuits are very complex. They need two stages and transformers, which lead to big size and high cost. In modern electronic devices, size and cost are critical, especially for portable devices. This is the motivation to propose another simple circuit for multilevel converter. It is easily obtained that the multilevel converter in the envelope amplifier system needs to have these characteristics:

- High efficiency
- Ability of fast output voltage change
- Without over-shoot or oscillation after the output step
- Good regulation under output current change

According to these features of multilevel converter, a multiphase buck converter is proposed in this thesis. In order to change the levels of the output voltage as fast as possible, the minimum time control strategy is applied during the voltage transition. On the other hand, at the constant voltage operation, PWM control is used.

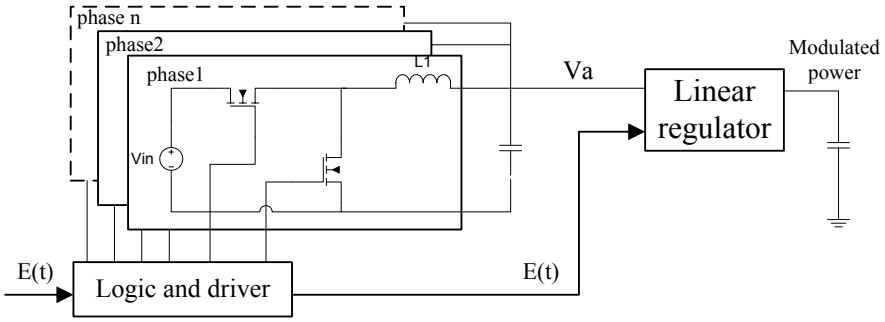

Figure 21: Multiphase buck converter in series with a linear regulator

As shown in Figure 21, the idea in this solution is to have the multiphase operating in open loop. Due to its open loop operation, it is a low cost solution because there are no voltage and current senses. The pre-defined discrete duty cycles are used for discrete output voltage levels, which are stored in a look up table. Thanks to the feature of interleaved multiphase converter, the duty cycles that have total ripple cancellation of the output voltage are selected, as shown in Figure 22. The reason for this selection will be explained in 3.2.1.

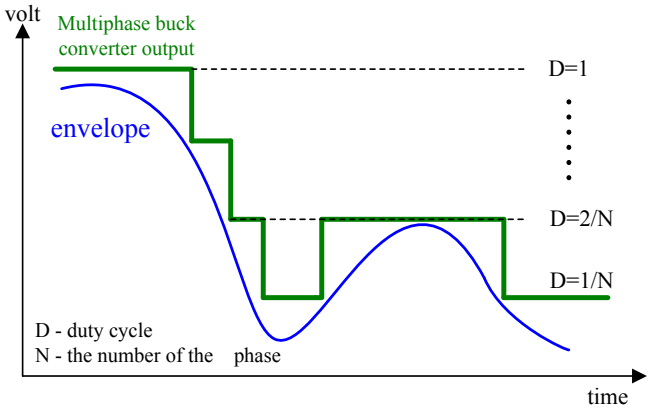

Figure 22: Time diagrams of the proposed solution

II.1 The proposed multilevel converter

Multiphase converter is widely used in microprocessor power supply and automotive applications in recent years. The advantage of multiphase

converter architecture is that it uses interleaved timing to multiply ripple frequency and in that way to reduce the input and output RMS currents. It means the ripple cancellation of input and output current ripple, which results in lower cost and value of output capacitors, small components and reduced the power dissipation. The peak-to-peak inductor current for individual phase can be calculated in Equation 7:

$$I_{PP} = \frac{(V_{IN} - V_{CC})V_{CC}}{L \cdot f_S \cdot V_{IN}} \tag{7}$$

Where, V_{IN} and V_{CC} are the input and output voltages, respectively. L is inductor value in each phase; and f_S is the switching frequency. *Figure 23* shows the ripple current on output capacitor in multiphase buck converter.

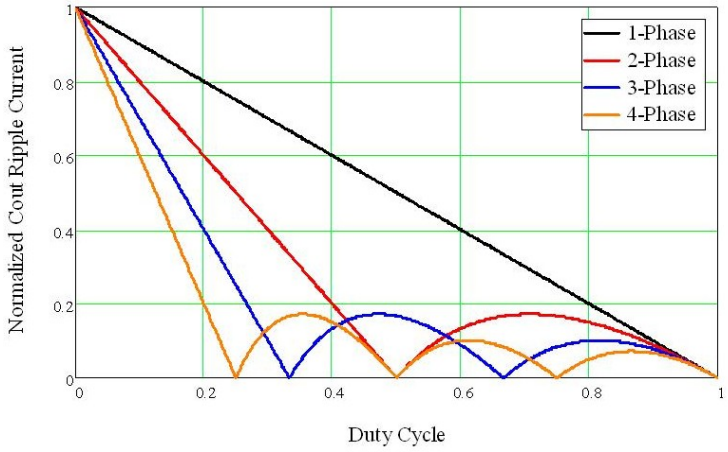

Figure 23: Output capacitor current ripple cancellation in multiphase buck converter

It should be noted that at the duty cycle that has value i/n (i=1, 2, 3…..n, n is the number of the phase), the ripple on the output capacitor can be totally cancelled and therefore, it can be very small (in theory there is no need to use it). As mentioned before, the solution proposed in this thesis uses these "Node" duty cycles. It means that all the inductor currents will flow to the load, which makes the output filter small and its design simple.

Another concern of the interleaved multiphase converters is current sharing. Most of the commercial converters solve this problem by including an additional current loop. As a consequence, the cost of the component is quite high, and also, it leads to the additional power losses and increasing size. Therefore, if the number of phases is high, the number of additional

component will be unacceptable. Since the solution in this thesis does not have any control loop in multiphase buck converter, the dc current sharing depends strongly on the conduction mode of the converter.

According to the investigation of current sharing in multiphase buck converter from the state of art [16], it indicates that the current unbalance in the phases mainly depends on the different value of dc parasitic resistance and the deviation of duty cycle. The worst case for a single phase takes place when this phase has the maximum duty cycle and maximum resistance. In that case, the phase current is the maximum above the average value I_{load}/N.

But the differences caused by resistance unbalance when only one resistance is different from the others (duty cycle is same in each phase) can be calculated as:

$$(\frac{\Delta I_i}{I_i})_R = -\frac{N-1}{N}\frac{\Delta R}{R} \tag{8}$$

R is the common resistance for the rest of the phases and ΔR is the difference in the unbalanced resistance. On the other hand, the differences caused by duty cycle unbalance when only one duty cycle is different from the others (parasitic resistance is same in each phase) can be calculated as:

$$(\frac{\Delta I_i}{I_i})_R = -\frac{N-1}{N}\frac{1}{1-\eta}\frac{\Delta d}{d} \tag{9}$$

The d is the common duty cycle for the rest of the phases, and Δd is the difference in the unbalanced duty cycle. The η is the power efficiency due to losses on the resistance exclusively.

The dc parasitic resistance is mainly caused by the series resistance of inductor, while the deviation of duty cycle is mainly caused by the deviation of the gate delay of the MOSFET. It is very difficult to exactly calculate the current distribution from the equations (8) and (9). However, a very important conclusion can be obtained from these equations is that the duty cycle is the most responsible for the main current unbalance unless the resistance causes very high losses (over 10%), which should be avoided by design. Regarding to the inductor value, the differences cause only unbalanced current ripples, but the dc current in each phase is unaffected. This feature of multiphase results in the problem in open loop design, because the gate delay deviation of MOSFET usually exists. Especially when the switching frequency is high, this problem is even more obviously.

However, thanks to high resolution digital control, it is possible to adjust the driving signal to achieve current sharing as much as possible without using current feedback.

The characteristics of multiphase buck converter used in this thesis can be summarized as:

- It operates in open loop
- There is not any current or voltage sense
- PWM only has discrete duty cycles d=i/n, i=1, 2, …n (n is the number of phases) in order to obtain total ripple cancelation
- It is necessary to considerate the filter design because of the trade-off between the efficiency and dynamics of output of the converter (it will be discussed in 3.1.4)

II.2 The Minimum time control

The multiphase buck converter has to be able to change output voltage very fast. In principle, the fastest way to have a step up voltage for a fixed synchronized buck converter is to keep the high side switch on and the low side one off. On the other hand, the fastest way to have a step down voltage is to keep the high side switch off and the low side one on. However, without accurate control, there will be over shoot and oscillations after the voltage step, which should be avoid in envelope amplifier application. Therefore, minimum time control is applied to achieve:

- Fast voltage step
- The voltage transition without over-shoot or oscillation after transition

The minimum time Principle

The minimum time control is base on Pontryagin's Minimum Principle. Its objective is to find the optimal control to transfer the system from a given initial state to a target state.

$$H(x^*(t),u^*(t),\lambda^*(t),t) \le H(x^*(t),u(t),\lambda^*(t),t) \tag{10}$$

Where x* is the optimal state trajectory, u* is the optimal control for the problem, and λ^* is the optimal costate trajectory [22].

Even more, the minimum time control indicates that transition between initial and target state can be in the minimum time by simply switching the control between the minimum and the maximum input value. It is not practical in all applications. However, the switching dc-dc converter is a very suitable system for the minimum time control, because the system's input always switches between its minimum and maximum value.

The implementation of the minimum time control is to recover from the load current step or to change the output voltage level through a single on-off action of power switches [23], as shown in Figure 24.

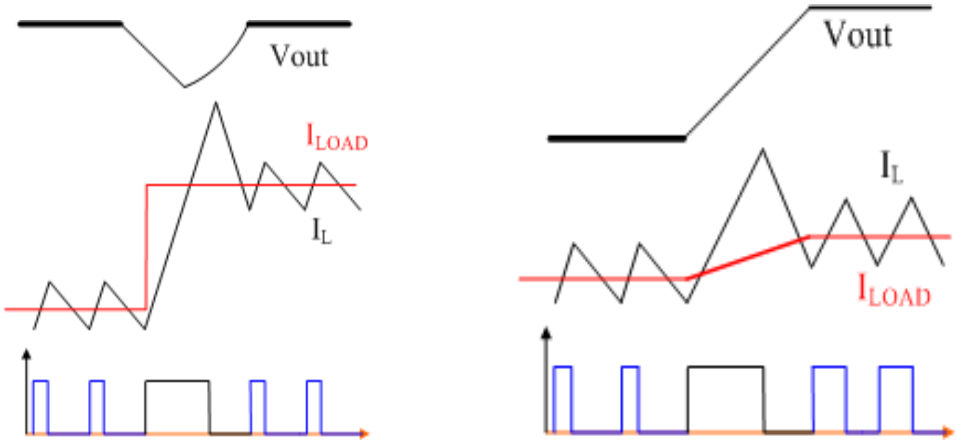

Figure 24: a single on-off action of power switches to recover from the load current step up (left) and to change the output voltage level

In order to obtain minimum time control response, there are two widely accepted methods, state-trajectory and charge balance. However, both methods still have some challenges of practical implementation.

State-trajectory

This method is based on a nonlinear behavior of power converter to achieve steady-state operation within one on-off switching cycle, regardless of the system's initial state or operating conditions [24]. The boost converter is simplest example to analysis the principle of this method. Figure 25 shows the schematic of a boost converter.

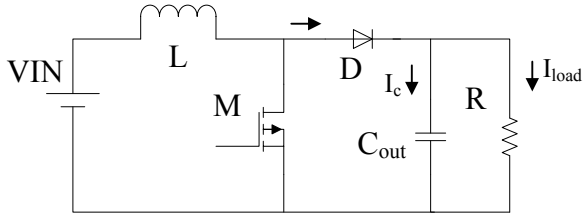

Figure 25: schematic of boost

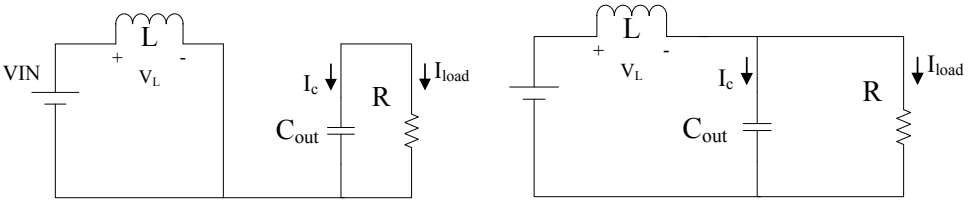

Figure 26: The equivalent circuit of main switch on and off

As shown in Figure 26, when the switch M is on and diode D is off. The inductor L is charging up with the input voltage V_{IN}. The output load R is supplied from the output capacitor C. the output voltage is Vo. Therefore,

$$VIN = L\frac{di_L}{dt} \tag{11}$$

$$i_C = C\frac{dv_o}{dt} = C\frac{dv_C}{dt} \tag{12}$$

When the switch M is off and diode D is on. The energy stored in L will release to the load and the capacitor. Therefore,

$$VIN - v_C = L\frac{di_L}{dt} \tag{13}$$

$$i_C = i_L - I_{OUT} \tag{14}$$

With (11) and (12), the normalized on-state equation can be obtained:

$$V_{CN} = -K_{1N}i_{LN} + K_{2N} \tag{15}$$

Where V_{CN} and i_{LN} are normalized capacitor voltage and inductor current respectively. K_{1N} and K_{2N} are parameters depending on input voltage and load current.

In the same way, with (13) and (14), the normalized off-state equation can be obtained:

$$V_{CN} = A_{1N} i_{LN}^2 + A_{2N} i_{LN} + A_{3N} \tag{16}$$

Where A_{1N}, A_{2N} and A_{3N} are parameters depending on input voltage and load current. And the state trajectories of boost converter can be drawn based on equation (15) and (16), as shown in Figure 27. Figure 28 shows the simplified application of the minimum time control based on state trajectories method.

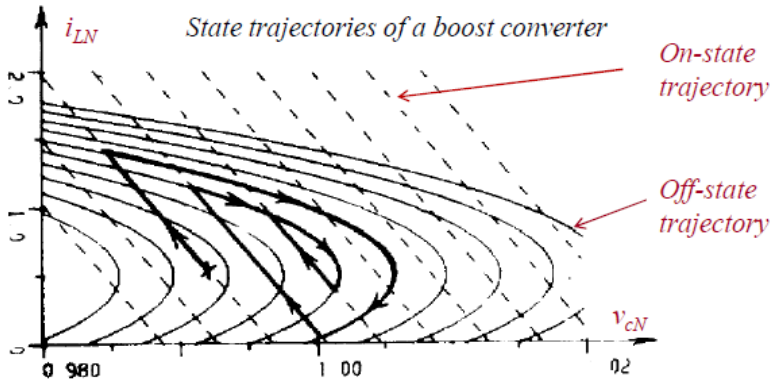

Figure 27: the boost converter state trajectories

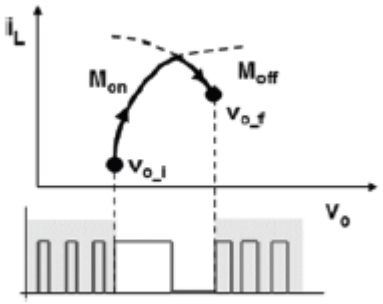

Figure 28: The implementation of state trajectories method for converter

Hysteretic control is a typical representative of this control method based on state-trajectory. However, there are some challenges for practical implementation.

- Complex derivation of the switching surface.
- Switching surface depends on the operating conditions (V_{in}, I_{out}).
- Requires fast sensing of inductor current.

Charge balance

The output voltage change results from the charge flowing in or out from capacitor [25]. During the steady state, the charge on the output capacitor keeps dynamically balance. Once the minimum time control is applied to the converter to change the output voltage level, the charge balance principle can be described by observing Figure 29 and Figure 30 showing a buck converter's output capacitor voltage and inductor current change during the minimum time control with resistor load and current source load respectively.

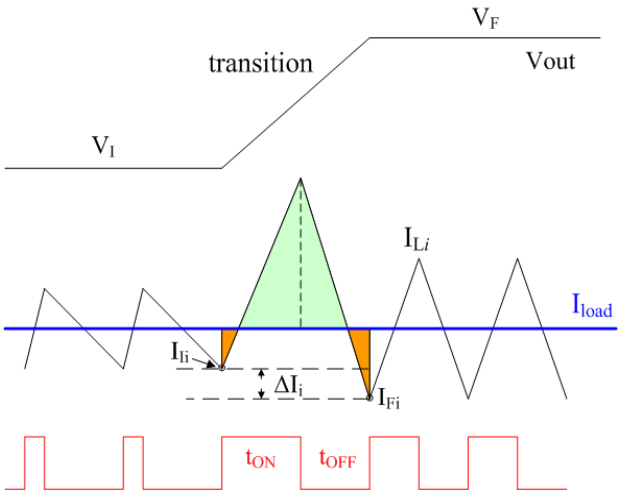

Figure 29: The charge balance with current source load

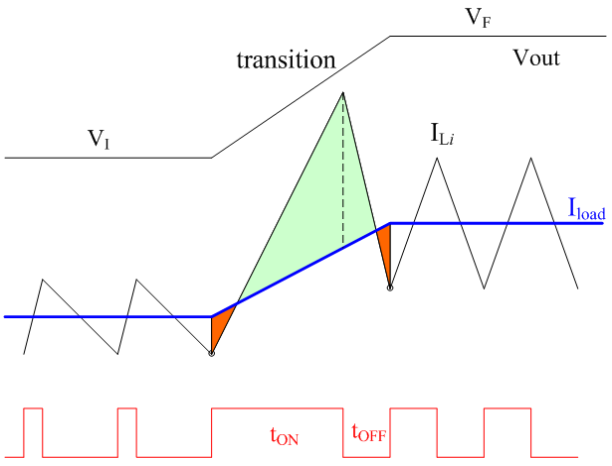

Figure 30: The charge balance with resistance load

The challenges of the practical implementation of charge balance method are:

- Detection of peak or valley point of inductor current.
- Accurate detection or calculation of inductor current ripple is required.
- The inductor slope depends on V_{IN}.

Comparing these two methods, the state-trajectory overlooks the inductor current ripples. However, when transition time is very small (such as one or two switching periods), the ripples are comparable with the peak value within transition time. In this case, the calculation will be inaccurate. In the proposed solution of this thesis, the transition time is expected as small as possible in order to track wide bandwidth envelope. Therefore, charge balance method is used in multilevel buck converter.

II.3 The control strategy in multiphase buck converter

The minimum time control has been applied to multiphase buck converter to recover output voltage from the load current step. The challenge in the proposed solution is that there are not output voltage and current feedback because of the open loop operation. However, thanks to the features of interleaved and ripple cancellation in multiphase buck converter, a control strategy for minimum time control regardless of the load current and output voltage detection is proposed in this thesis.

In order to calculate the minimum time and the intervals during which the main switch in the buck converter is turned on and off in multiphase buck converter, it is necessary to analyze the charge flow in each one phase of the multiphase buck converter. The assumption that the output voltage changes linearly during the transient is made:

$$V_{\text{out}}(t) = V_1 + \frac{\Delta \text{V}}{\Delta t} t \tag{17}$$

Where V_1 is the buck's output voltage before the transient starts, Δt is the duration of the transient and ΔV is the voltage difference of the output's voltage after and before the transient. During the transient time, from initial voltage (V_1) to the final voltage (V_2), the output capacitor will receive the charge of

$$Q_{\mathrm{C}} = \mathrm{C}(\mathrm{V}_2 - \mathrm{V}_1) = \mathrm{C} \cdot \Delta \mathrm{V} \tag{18}$$

where C is the value of the output capacitor. During the same time the load will receive the charge of:

$$Q_{\mathrm{LOAD}} = \mathrm{I}_{\mathrm{LOAD}} \cdot \Delta \mathrm{t} \tag{19}$$

Here it is assumed that the load is a current source (if the load is a linear regulator and the voltage change is sufficiently fast so that the load's current is constant, i.e. the envelope is not changed significantly). All that charge will come from the converter's inductors and it can be calculated as:

$$\sum_{\mathrm{i=1}}^{\mathrm{N}} Q_{\mathrm{Li}} = \mathrm{Q}_{\mathrm{C}} + \mathrm{Q}_{\mathrm{LOAD}} \tag{20}$$

where QLi is the charge provided by each phase of the multiphase converter. If it is assumed that the voltage change is linear, which is close to the actual response, the charge of one phase, QLi, can be calculated as:

$$Q_{Li} = I_i \Delta t - \frac{V_{in}}{2L} t_{ON,i}^2 - \frac{V_1}{2L} \Delta t^2 + \frac{V_{in} t_{ON,i} \Delta t}{L} - \frac{\Delta V \Delta t^2}{6L} \tag{21}$$

where Ii is the ith inductor's current before the transient, $t_{ON,i}$ is the time interval during which the main switch of the ith phase is turned on and L is the value of the inductor in each phase. It can be seen that the charge through each phase depends on the current through each phase before the transient. When the equation (21) is substituted in equation (20) it is clear that the total charge depends on the sum of the phase currents. If the duty cycle of the multiphase converter is chosen as i/n (i=1…n, n is the number of the converters) the sum of phase currents is always equal to the load's current, otherwise there will always be a small portion of the current that goes to the capacitor due to the voltage ripple. Therefore, by selecting the duty cycles of i/n not only the output voltage has lower ripple, but the calculation of the transient time is more exact.

For each phase it can be written:

$$L \Delta I_i = V_{in} t_{on,i} - V_1 \Delta t - \frac{1}{2} \Delta V \Delta t \tag{22}$$

where ΔIi is the difference of the phase current after and before the transient (Figure 31). Equation (22) leads to

$$t_{on,i} = K \Delta t + \frac{L \Delta I_i}{V_{in}}, \quad K = \frac{V_1 + \frac{\Delta V}{2}}{V_{in}} \tag{23}$$

$$t_{on,i}^2 = K^2\Delta t^2 + \frac{L^2\Delta I_i^{\,2}}{V_{in}^2} + \frac{2KL}{V_{in}}\Delta t\Delta I_i \tag{24}$$

It can be shown that for the selected duty cycles the following equation always holds that

$$\sum_{i=1}^{N}\Delta I_i = 0 \tag{25}$$

Combining equations (23-25) it can be obtained:

$$\sum_{i=1}^{N} t_{on,i} = nK\Delta t \tag{26}$$

$$\sum_{i=1}^{N} t_{on,i}^2 = nK^2\Delta t^2 + \frac{L^2}{V_{in}^2}\sum_{i=1}^{N}\Delta I_i^2 \tag{27}$$

Since the parameters of the converter and the transient voltages (V_1, V_2) are known, $\sum_{i=1}^{N}\Delta I_i^2$ can be calculated. By using (20), (21), (26) and (27), the following equation is obtained:

$$C\Delta V + I_{load}\Delta t = \Delta t^2\left(-\frac{V_{in}}{2L}nK^2 + \frac{V_{in}}{L}nK - \frac{V_1}{2L}n - \frac{\Delta V}{6L}n\right) + \Delta t I_{load} - \frac{L}{2V_{in}}\sum_{i=1}^{N}\Delta I_i^2 \tag{28}$$

From this quadratic equation, the transition time, Δt, can be calculated and then the turn on interval of each phase is obtained by using (23).

It is important to notice that the transition time in equation (28) does not depend on the load current, but only on the difference of the current. Even more, it can be seen that the current unbalance in the phases does not affect the calculation of the transition time. Taking advantage of this feature, the open loop design of the multiphase converter becomes feasible [26].

Figure 31 shows one voltage transition and one phase current. Some of the earlier mentioned values like ΔIi or Ii can be observed.

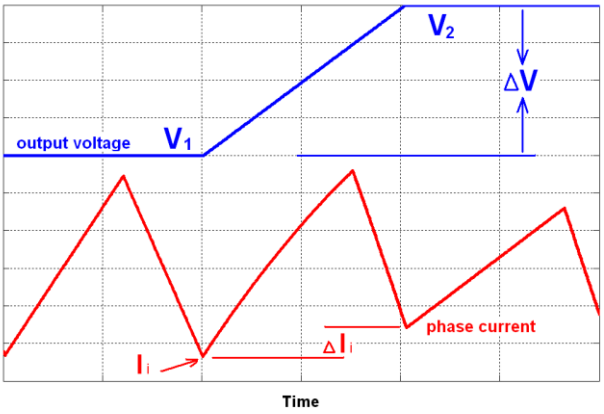

Figure 31: Simplified waveforms of the buck's output voltage and the current through one phase.

The characteristics of the minimum time control strategy can be concluded as:

- A single on-off action of power switches for each phase respectively
- Charge balance principle
- Control parameters (ton and toff) can be calculated and stored in look-up table
- Duration of the minimum transition time is fixed by filter and the voltage before and after the transition

According to the analysis above, the important conclusions of the proposed minimum time control strategy are:

- The transition time algorithm does not depend on the load current
- The current unbalance in the phases does not have influence during the transient
- The output filter can be designed in such a way that it is possible to obtain voltage transition as fast as one switching cycle or even faster

II.4 The filter design consideration

As mentioned earlier, the "Node" operation points result in simple filter design, because of the ripple cancellation. However, the minimum transition time depends on the filter obviously through the analysis above.

For the given filter parameters (L, C), the transient time can be calculated. This transient time restrict the maximum frequency of the envelope that the converter can modulate. However, the design way is usually inversed. The maximum transient time is fixed by the application, then there are a plenty of possibilities for the filter parameters (L, C). The inductor limits the slew rate of current through the output capacitor, and the output capacitance value determines the charge that has to be delivered during the transient time to change the output voltage. Designing for very fast output voltage transient, a high ratio between L and C is suitable for charging output capacitor very fast. And it makes inductor size large. But the good regulation under the load current change requires a low ratio between L and C. It reduces the size of inductor, but increase the inductor current ripple, which leads to increased power losses in the inductor.

If the maximal slope of the envelope signal is known the selection of the L and C can be made by using this information and the equations from section 3.1.3. It can be shown that there is a following relationship between the converter's parameters:

$$C < \frac{\Delta V}{6Lm^2}(6V_{in}nK - 3nV_1 - n\Delta V - 3nK^2V_{in}) - \frac{L}{2V_{in}\Delta V}\sum_{i=1}^{N}\Delta I_i^2 \qquad (29)$$

where m is the maximal slew rate of the buck's output voltage. Figure 32 shows the constraint of the filter to track the maximum envelope slope of 52.4 volts/us for OFDM signal. The combinations of L, C and f_{SW} on the surface are the minimum requirement in order to track that envelope.

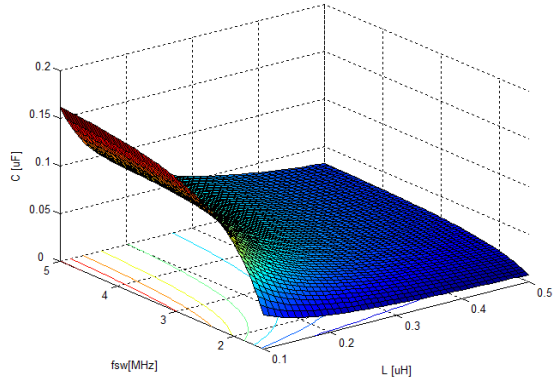

Figure 32: a constraint of the filter design from output 3V to 9V

III. The envelope amplifier for EER based on the proposed multilevel converter

The multilevel converter can only generate discrete levels voltage. A linear regulator is used as low pass filter in order to have output voltage tracking the envelope reference in EER. This linear regulator is not necessary in ET, because the multilevel converter just provides the modulated power supply. Figure 33 shows the schematic of the envelope amplifier.

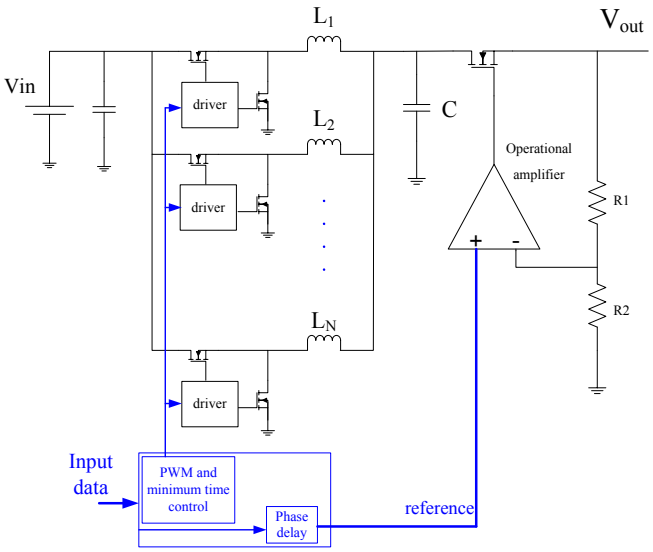

Figure 33: Simplified schematic of the integration of envelope amplifier

As it has been mentioned earlier, the bandwidth of this envelope amplifier is limited by the bandwidth of the linear regulator. Therefore, the MOSFET, operational amplifier and components that operate at high speed should be chosen for the linear regulator. Also the maximum operation voltage is important, and it has to at least equal to the highest level output of multilevel converter.

In order to obtain a wide bandwidth, the MOSFET's input capacitance should be as low as possible. Hence, the possible candidates for the MOSFET have been selected from HF/VHF power MOS transistors. The input capacitance of these transistors is in order of hundreds of pF. Another reason for the selection of low input capacitance is due to the control of the MOSFET. It is controlled directly from the output of the operational amplifier

and, therefore, the lower the capacitance between MOSFET's gate and source, the better, because a high capacitance can lead to the current saturation of the operational amplifier's output. Additionally, if the input capacitance is comparable with the output capacitor of multiphase buck converter, this capacitance has to be taken into account in the calculation of minimum time control.

The digital control component can be a FPGA or DSP. All the discrete duty cycle value and the minimum time control parameters are pre-defined and stored in the look-up table. The advantage is that all the control can be integrated into the same FPGA or DSP with digital signal of power amplifier. That would be an easily implementation and low cost solution. From the integration schematic, it can be seen that the reference to the linear regulator should be delayed comparing with the reference to the multilevel converter. The reason of that delay is the feature of the minimum time control, and the detail will be explained in the next chapter.

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Chapter4. Implemented EER envelope amplifier

The idea for the proposed envelope amplifier is verified with a 4-phase buck converter prototype. The minimum time control is implemented in a DSP and an FPGA respectively.

I. The minimum time control in a 4-phase buck converter

The equations to calculate on and off time are shown in 3.1.3. However, it can be found that the parameters ΔIi that are needed to calculate on and off time are still unknown. In order to know these parameters, we proposed a control strategy that is to synchronize the minimum time control with PWM signal. In that way, ΔIi of each phase can be exactly calculated through input voltage, duty cycle and inductance. This control strategy is shown in Figure 34. When the envelope reference crosses one voltage level, the output voltage should be changed to a higher level by applying the minimum time control and changing the duty cycle. However, the transition will not start immediately, instead it will wait for a rising edge of any phase's PWM signal. For example, Figure 34 shows the control of transition from duty cycle 0.25 to 0.5. At the moment of the rising edge of PWM of the first phase, all the phases enter the minimum time control. Each phase will have different t_{ON} and t_{OFF} time from the calculation, but the total transition time (t_{ON}+ t_{OFF}) is the same. After the transition time, all the phases have to continue the PWM signal with new duty cycle and its corresponding phase delay. The strategy is that the phase whose rising edge of PWM signal is synchronized with the minimum time control will continue with the rising edge of the new PWM signal and all the other phases keep the same phase delay just like before the transient. The actuation of this control strategy can be seen from Figure 35, where the simulation results of inductors current and output voltage are presented. If the current in the phases is balanced before the transition, the currents will be balanced after as well.

On the other hand, for the step down transition of output voltage the difference is that the minimum time control is synchronized with the falling edge of PWM signal.

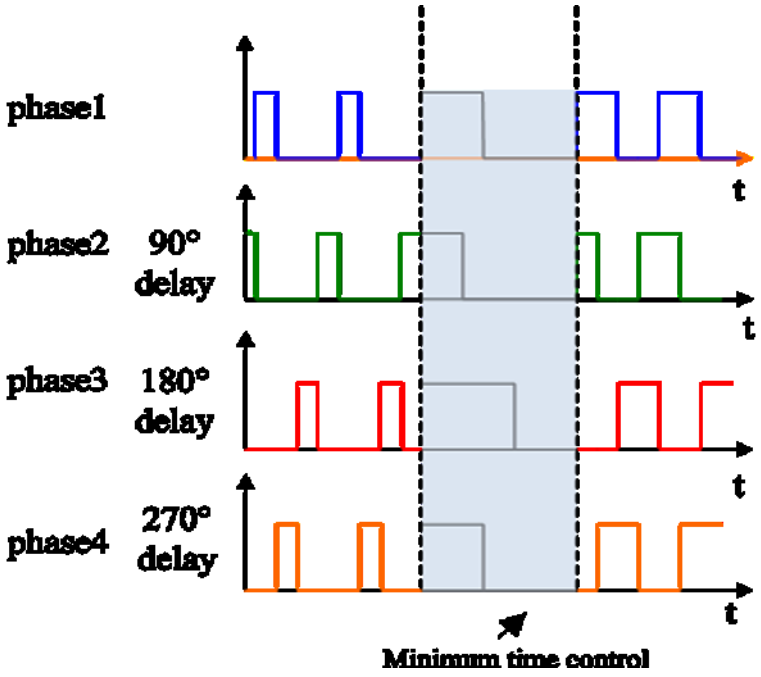

Figure 34: Control strategy for the voltage transition from $0.25V_{IN}$ to $0.5V_{IN}$

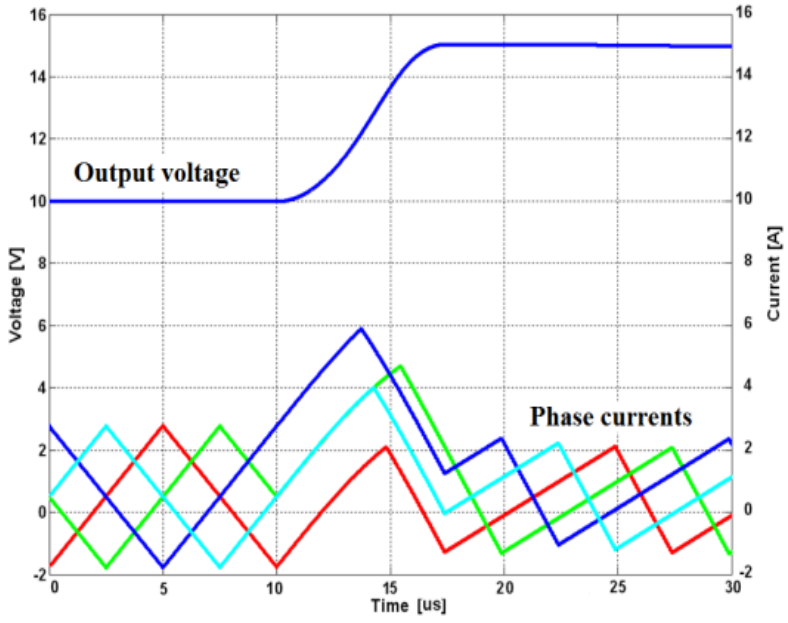

Figure 35: Simulation results for the voltage transition from $0.25V_{IN}$ to $0.5V_{IN}$

The characteristics of this control strategy can be concluded as:

- The start of transition is synchronized with the raising edge or falling edge of the PWM.
- Different $t_{ON,i}$ and $t_{OFF,i}$ are applied to each phase, but the same Δt for each phase.
- After the transition the phases maintain the synchronization.

II. The first prototype

A 4-phase buck converter is implemented as the first prototype just to verify the minimum time control strategy proposed in this thesis. The parameters of this multiphase buck converter are as follows:

- Input voltage of 20V
- The discrete output voltage level are 5V, 10V and 15V
- The switching frequency is 100kHz
- Inductance for each phase is 11uH
- Output capacitor is 11uF

For the drivers and MOSFETs, IR2110S and IRL5N are used respectively. The minimum time control strategy is implemented with DSP, Piccolo MCU controlSTICK Tool, which has 4 PWM generators with interleaved configuration.

Figure 36 shows the output voltage transition from 5V to 10V (25% duty cycle to 50% duty cycle). It is verified from the result that the minimum time control strategy we propose does not depend on the load current, just like it is anticipated in the theory (section3.1.3). In Figure 36, the load currents are 1A and 2A respectively, and the same t_{ON} and t_{OFF} times are applied. It can be seen that the transition time is only around 1.6 switching period and there are no over shoot and oscillations. Additionally, it is not necessary to know the inductor current value before and after the transition, but to know the difference of the current is enough because of the total ripple cancellation. The continue voltage steps of the implemented converter is shown in Figure 37.

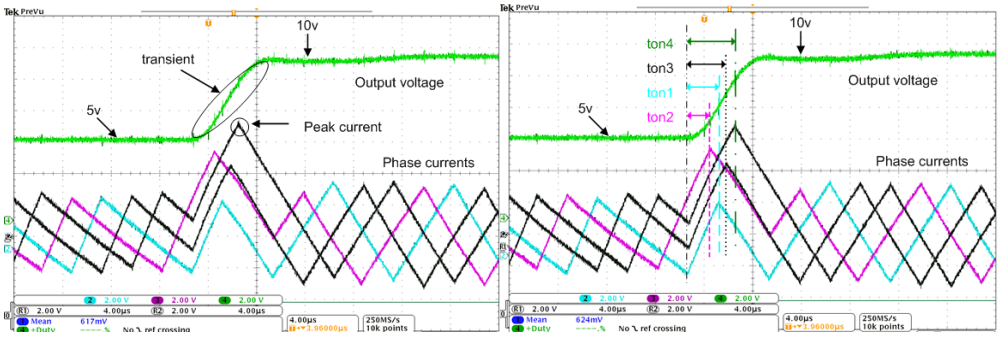

Figure 36: Output voltage step from 5V to 10V at 1A (left) and 2A (right) load current, 100kHz

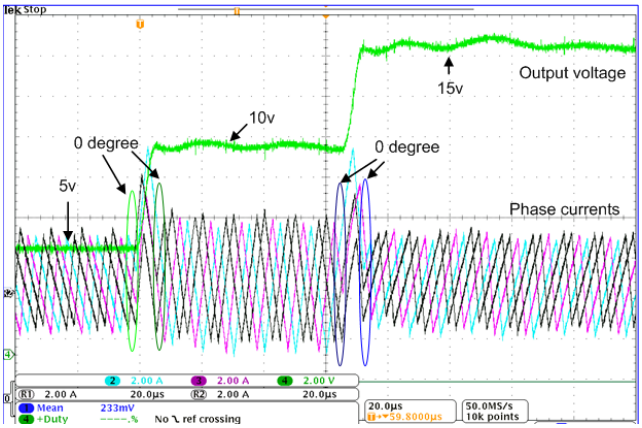

Figure 37: Output voltage step from 5V to 10V and from 10V to 15V at 1A load, 100kHz

III. The second prototype

In order to apply the proposed solution to the RF application, it is necessary to improve the switching frequency and reduce the voltage transition time. The goal is to integrate the multilevel converter with linear regulator and to test the behavior of the proposed envelope amplifier.

III.1 The control implementation in an FPGA

Due to the fast output voltage transition, high resolution of digital control is required to apply the minimum time control precisely. Therefore, FPGA

(Spartan-3) is used for the second prototype's controller. Figure 38 shows the control scheme of the proposed strategy.

The envelope reference is the input of this control and the outputs are drive signals of each MOSFET. All the parameters for possible transition that are needed for the minimum time control ($t_{ON,1}$, $t_{ON,2}$, $t_{ON,3}$, $t_{ON,4}$,Δt) are stored in the memory. The duty cycle depends on the level of the envelope reference through the quantization block, which works like an A/D converter. In order to apply the control shown in Figure 33, there are four independent counters for PWM generators. When the converter operates in steady state, the outputs of controller are the outputs of PWM generators. Once the duty cycle changes, the state machine that is in the PWM_state waits until there is rising edge (for step up) or falling edge (for step down) coming from any phase. At this moment, the state machine enters into Non_PWM_state, also the values of the counters are stored in the register and all the phases start the minimum time control. During the Non_PWM_state, the parameters in the look up table are used to apply t_{ON} and t_{OFF} for each phase independently. Having in mind that all phase have the same Δt, therefore, all the phases quit from the minimum time control at the same time. At this moment, all the counters are reset by the values that are already stored in the register before the minimum time control, and the PWM generators take the output of the controller again.

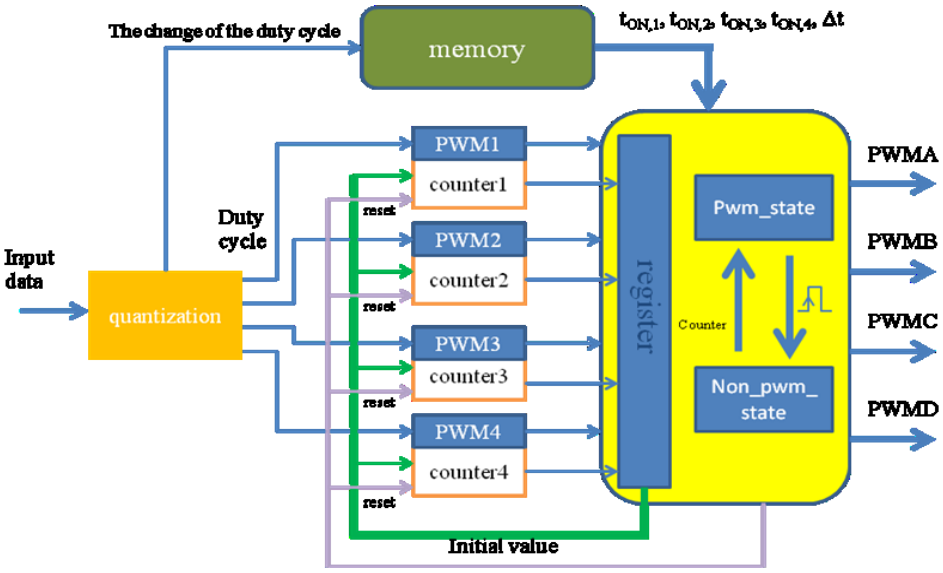

Figure 38: The control scheme in FPGA

Table 1different transient time from calculation

Transient	Phase	t_{ON} [ns]	t_{OFF} [ns]	Δt [ns]
From 0.25VIN to 0.5VIN	1st	628	1132	1760
	2nd	556	1194	1760
	3rd	754	1006	1760
	4th	691	1069	1760
From 0.5VIN to 0.75VIN	1st	1131	629	1760
	2nd	1194	566	1760
	3rd	1006	754	1760
	4th	1069	691	1760
From 0.75VIN to VIN	1st	2175	204	2379
	2nd	2133	246	2379
	3rd	2050	329	2379
	4th	1988	391	2379
From VIN to 0.75VIN	1st	204	2175	2379
	2nd	246	2133	2379
	3rd	329	2050	2379
	4th	391	1988	2379
From 0.75VIN to 0.5VIN	1st	629	1131	1760
	2nd	566	1194	1760
	3rd	754	1006	1760
	4th	691	1069	1760
From 0.5VIN to 0.25VIN	1st	1132	628	1760
	2nd	1194	566	1760
	3rd	1006	754	1760
	4th	1069	691	1760

Table 1 shows calculation results for this prototype, which are stored in the FPGA's memory. From these results, it can be seen that the high resolution control is required. Therefore, the DCM module in Spartan-3 is used in order to have up to 200MHz clock frequency.

III.2 The implementation of multilevel converter and experimental results

The parameters of the second prototype are as follows:

- Input voltage of 12V.
- The discrete output voltage level is 3V, 6V, 9V and 12V
- The switching frequency is 1MHz
- Inductance for each phase is 6.8uH
- Output capacitor is 1uF

LM2722 is used as a high frequency driver and N channel MOSFET SI4840BDY from VISHAY SILICONIX is used as switching devices. We use 10 ohms resistor as load and the idea is to have 10 watts of peak power. As mentioned earlier, because of high resolution for the minimum time control, an FPGA is used to control the converter. The FPGA clock is 50MHz and the clock can be boosted to 200MHz with DCM module. Therefore, we can control the time with the resolution of 5ns and previously used DSP has the time resolution of 100ns that is not sufficient for this application. Figure 39 shows the output voltage transition from 3V to 6V (25% duty cycle to 50% duty cycle). It can be observed that the output of the converter changes from one steady state to another steady state without over-shoot and oscillation by applying the proposed control strategy. Additionally, the current unbalance in the phases does affect the transition, which can be observed from Figure 39. Figure 40 shows the step down transition from 9V to 6V (75% duty cycle to 50% duty cycle). It can be seen that the transition time is only around 1.5 switching period. Figure 41 shows the behavior of multilevel converter with sinusoidal signal as input envelope reference. Table 2 shows the experimental transient time. Comparing with Table 1, there are some differences, because the model that is used for the calculation is idea one and it introduces some slight errors. However, it still makes a good starting point

to find real transient time. The efficiency of the converter is measured shown Figure 42. With this measurement, the whole envelope amplifier's efficiency can be estimated around 60%. The photo of the 4-phase buck converter prototype is shown in Figure 43.

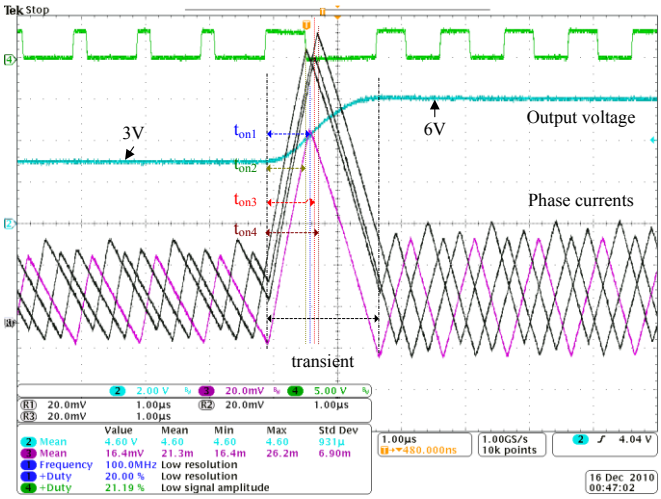

Figure 39: Output voltage step from 3V to 6V, 1MHz (2V/div) and Phase currents (200mA/div)

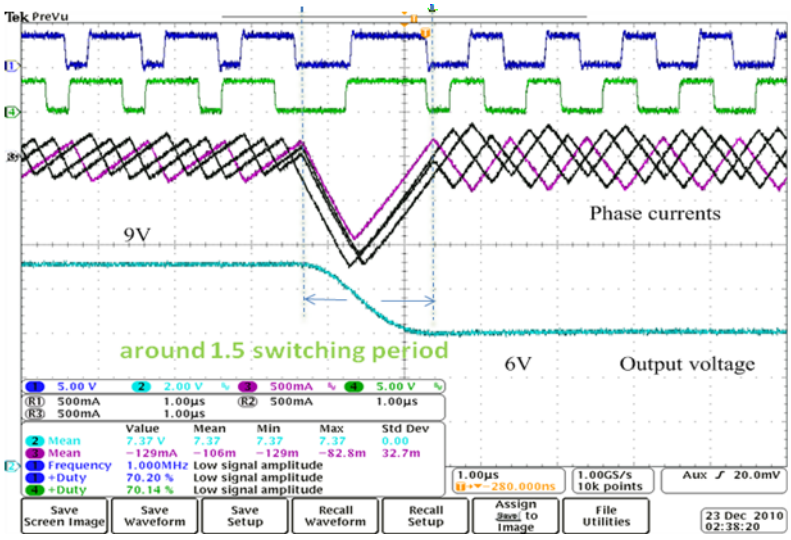

Figure 40: Output voltage step from 9V to 6V, 1MHz (2V/div) and Phase currents (500mA/div)

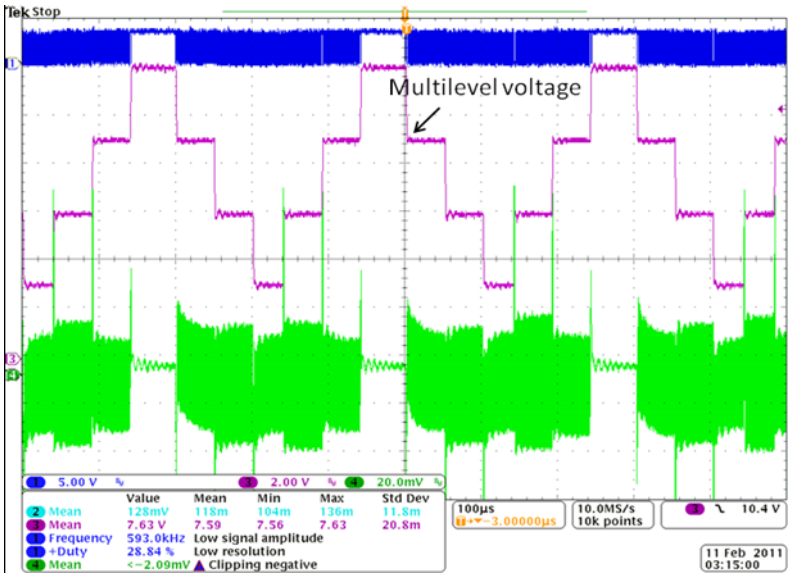

Figure 41: The waveform of multilevel converter with sinusoidal reference

Table 2 different transient time from experiment result

Transient	Phase	t_{ON} [ns]	t_{OFF} [ns]	Δt [ns]
From 0.25VIN to 0.5VIN	1st	628	1102	1730
	2nd	566	1164	1730
	3rd	754	976	1730
	4th	691	1039	1730
From 0.5VIN to 0.75VIN	1st	1131	629	1760
	2nd	1194	566	1760
	3rd	1006	754	1760
	4th	1069	691	1760
From 0.75VIN to VIN	1st	2000	190	2190
	2nd	1820	370	2190
	3rd	1870	320	2190

	4th	1810	380	2190
From VIN to 0.75VIN	1st	260	1840	2100
	2nd	460	1640	2100
	3rd	390	1710	2100
	4th	450	1650	2100
From 0.75VIN to 0.5VIN	1st	730	990	1720
	2nd	670	1050	1720
	3rd	860	860	1720
	4th	795	926	1720
From 0.5VIN to 0.25VIN	1st	1180	550	1730
	2nd	1240	490	1730
	3rd	1055	675	1730
	4th	1115	615	1730

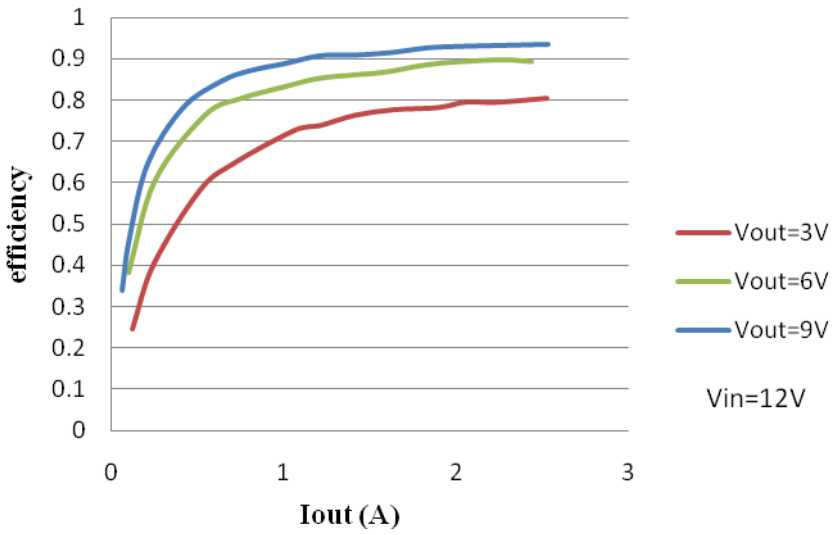

Figure 42: Efficiency of the multiphase buck converter

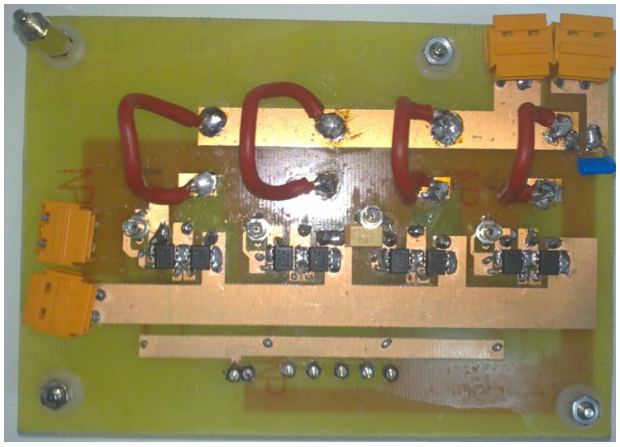

Figure 43: The prototype of the 4-phase buck converter

III.3 The linear regulator

As mentioned earlier, a linear regulator is used in series with the multilevel converter as the post regulator. Figure 44 shows its schematic.

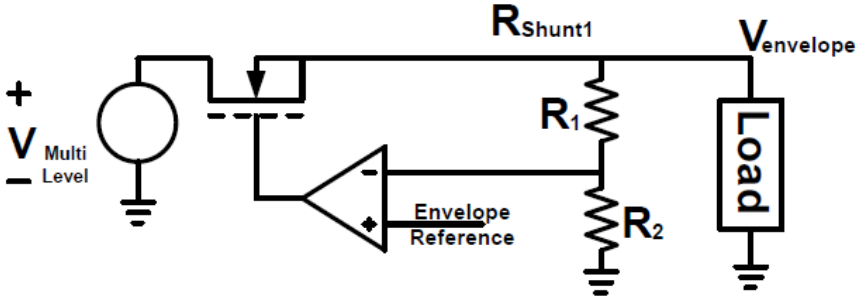

Figure 44: Simplified schematic of the implemented linear regulator.

The main components of the linear regulator in the prototype are as follows:

- A MOSFET BLF177 as the pass element
- An operational amplifier LM6172 for the feedback

The bandwidth of the linear regulator can be obtained from the open loop gain of the operational amplifier and the voltage divider with resistances R1 and R2, which is approximately 6MHz.

III.4 The envelope amplifier experiment

Figure 45 shows the output of multilevel converter and output of the envelope amplifier with 5kHz sinusoidal signal as the envelope reference.

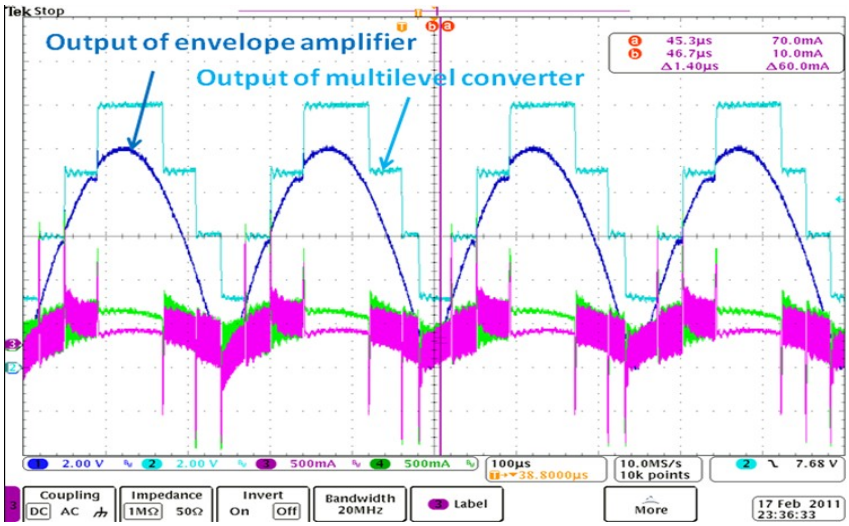

Figure 45 Output of envelope amplifier and multilevel converter of the proposed solution

The sinusoidal signal is generated through the memory in FPGA. This signal is both the envelope reference for multilevel converter and reference for linear regulator. Therefore, it is necessary to use a D-A converter for the linear regulator reference. The currents of inductor show that there is different DC resistor value in the phases, but it does not affect the transition. However, as mentioned earlier, the current unbalance caused by parasitic DC resistor value leads to low efficiency. It can be seen that the delay between two references is needed because the transition has to be synchronized with the PWM signal as we mentioned before. Figure 46 shows the result of envelope amplifier with that delay, which uses 20kHz reference. The measured efficiency is up to 80%. The result with 50kHz reference is shown in Figure 47. The strategy is that it only uses two discrete levels (50% duty cycle and 100% duty cycle), which takes advantage of this control method. The efficiency of envelope amplifier with this reference has been measured as 76.5%. Both 20kHz and 50kHz reference measurements use 10 ohms resistor load. Figure 48 shows the complete prototype of the proposed envelope amplifier. This delay problem can be fixed by including the registers in the envelope reference to the linear regulator.

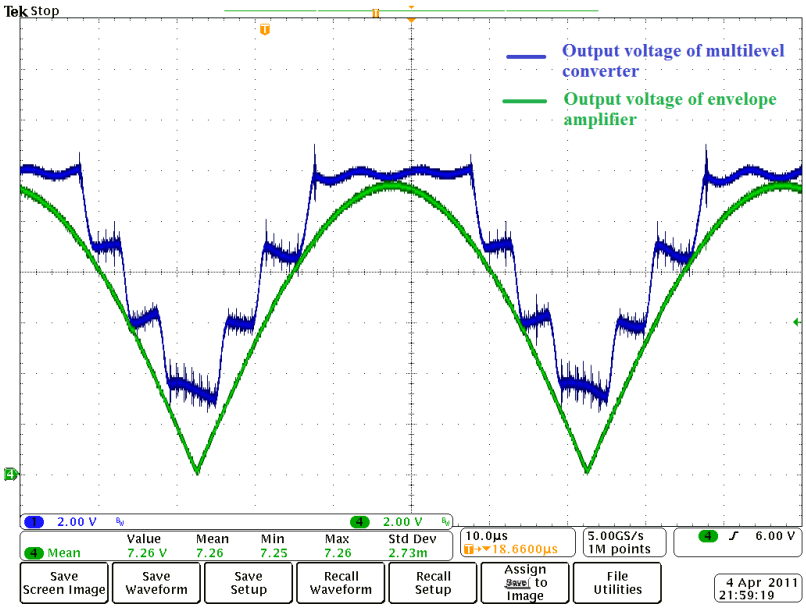

Figure 46: Output voltage of multilevel converter and envelope amplifier with 20kHz reference

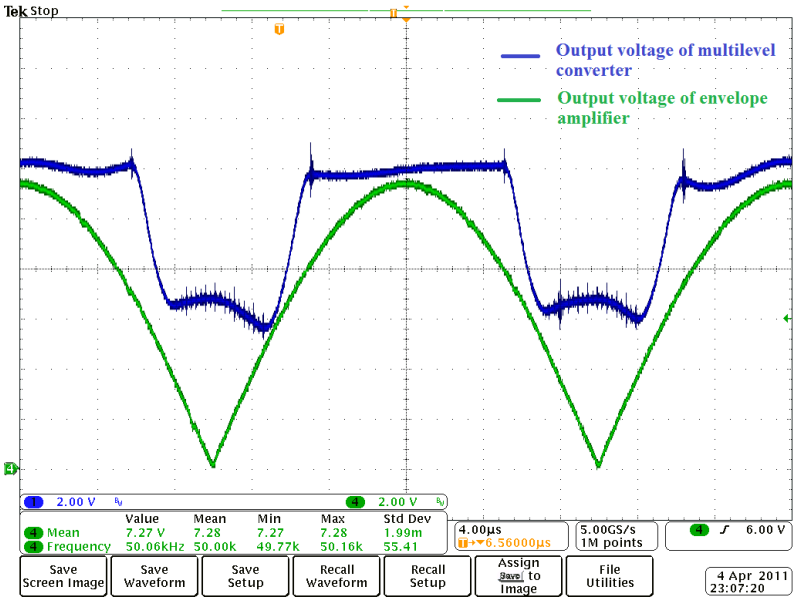

Figure 47: Output voltage of multilevel converter and envelope amplifier with 50kHz reference

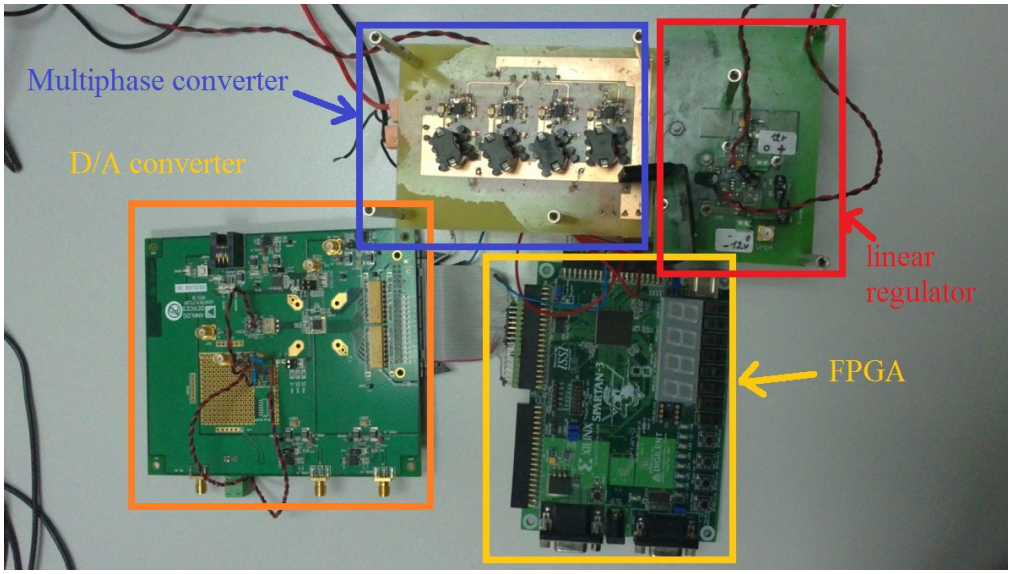

Figure 48: the envelope amplifier prototype

Chapter5. Conclusions and future work

Conclusions

An envelope amplifier solution based on multiphase buck converter with the minimum time control is presented in this thesis. The multiphase buck converter behaves as a converter with multilevel output voltage. The minimum time control is applied to change the output voltage of the converter as fast as possible. The advantage of this idea is to have trade-off the efficiency and the bandwidth of envelope amplifier. Since the multiphase buck converter does not need to have output voltage exactly track the envelope, the switching frequency can be relatively low that means low switching losses. On the other hand, the bandwidth of envelope amplifier depends on the bandwidth of linear regulator and the linear regulator inherently has high bandwidth and high linearity which are important for envelope tracking.

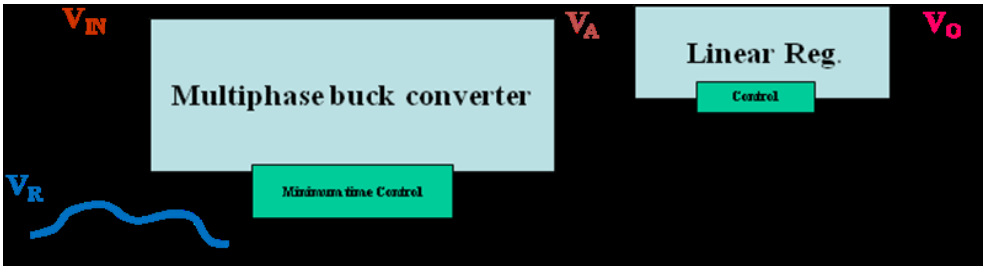

Figure 49: Block diagrams of the proposed solution

The multiphase buck converter in this solution operates in open-loop. There are not voltage and current loop, which means fewer components and low cost. And the important feature for this multiphase buck converter is that it works in the "Node", the total ripple cancellation duty cycles. This reduces the complexity of filter design, because there is no ripple on output capacitor. However, the objective of this design is to improve the system efficiency, therefore, the optimization efficiency of converter itself is also important. The trade-off of inductance is that low inductance means fast transition time but high ripple of the current in the inductor that leads to high core losses.

The minimum time control principle indicates that the switching dc-dc converter can change from one steady state to another by applying a single on-off action of power switches within minimum time, based on charge balance method. With this principle, we propose a minimum time control strategy for multiphase buck converter that operates in "Node" to change the output voltage between discrete levels. Taking the linear regulator as load of the converter into account (the linear regulator behaves as current source), the advantages of this control strategy are as follows:

- No need to know the load current
- The current unbalance in the phases does not affect the transition

These features make the open loop operation become feasible. The theory is validated by experiment results, which show that there are no over-shoot and oscillation between two steady states. This control strategy design is the main work of this thesis.

The advantages of this solution can be concluded as:

- Very simple circuit and easy implemented control
- Small spectrum interference with the output spectrum (because there is no overshot or oscillation after the transition)
- The trade-off between switching frequency and fast envelope tracking

The limitations of this solution also have to be mentioned. The first is that the current balance in multiphase buck converter can't be guaranteed because of the open loop operation. The second is high resolution control requirement, especially when the transition time is very small. The third is regarding to the efficiency optimization. The output voltage has fixed levels because of the "Node" duty cycles. It restricts this solution to have adjustable output voltage level in order to optimize the efficiency of envelope amplifier depending on the envelope reference [21].

Future work

As a solution for RF application, high bandwidth of the envelope amplifier is critical. The second prototype still can only track very low frequency envelope, which can be seen from the experiment results. However, one of the important things of this thesis is that we propose a concept for the minimum time control applying on multiphase converter and for multilevel

converter solution. However, to transfer the concept to real application, there are still plenty of works that can be addressed:

- Investigate the bandwidth limitation of envelope amplifier due to the inherent drawback of this solution.
- The efficiency and linearity measurement of the whole PA system. These are main targets of the design.
- Design of the number of multiphase buck converter in order to have efficiency design.
- Consideration of other possible applications of the proposed control strategy such as DVS.

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