CEI UPM
Centro de Electrónica Industrial

Centro de Electrónica Industrial

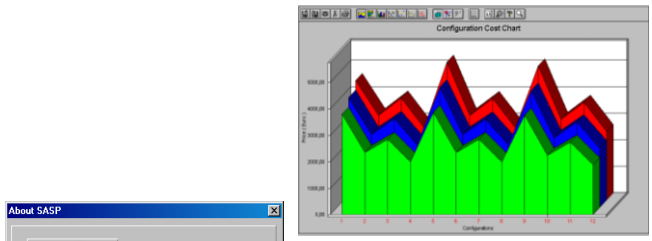
cei@upm.es

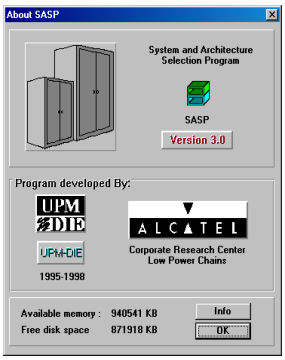
Power Electronics Modeling Activities

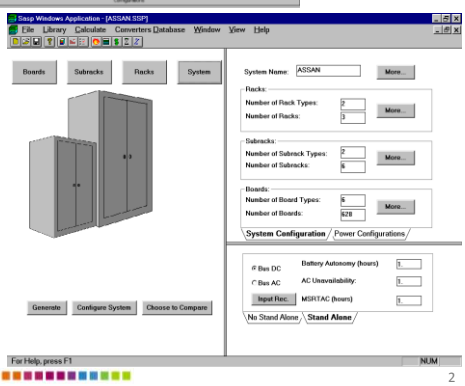
UNIVERSIDAD POLITÉCNICA DE MADRID

POLITÉCNICA

Sasp



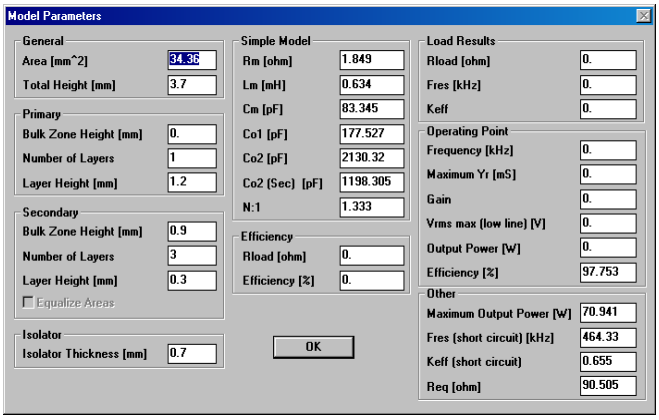




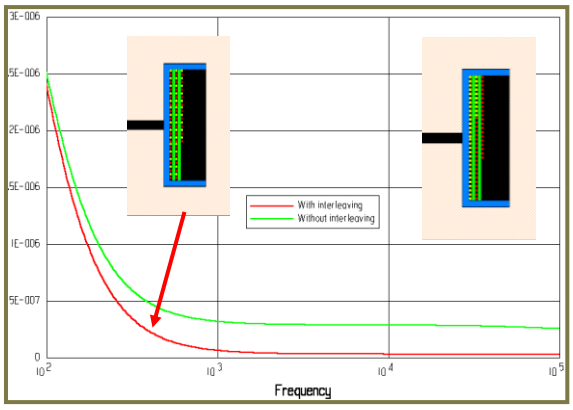
CEI UPM

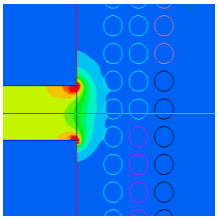
POLITÉCNICA

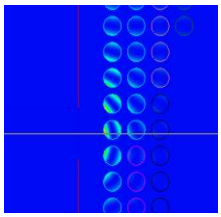
PTModel



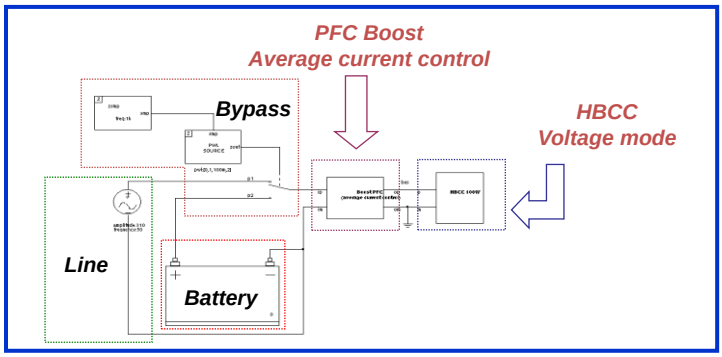
Powercad



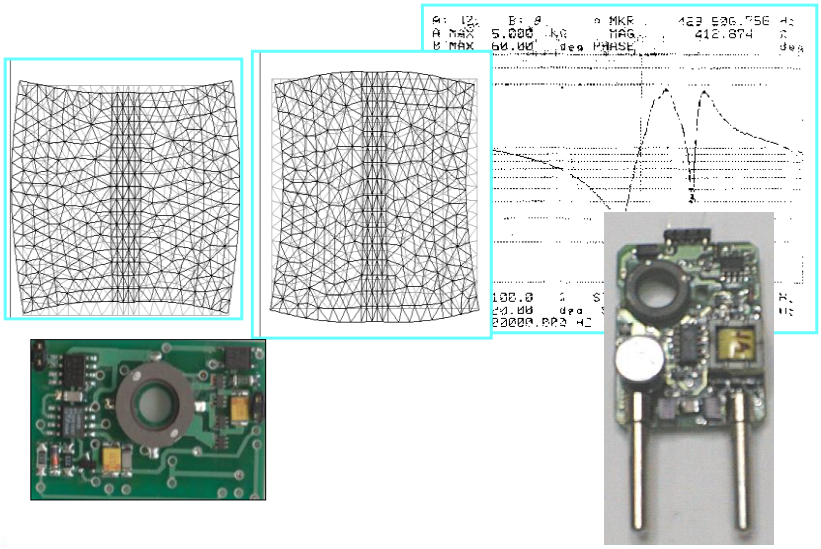




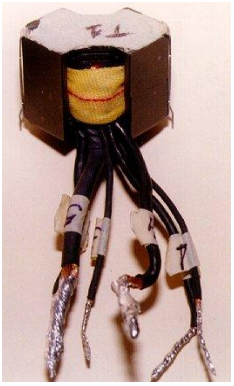
PowerSim

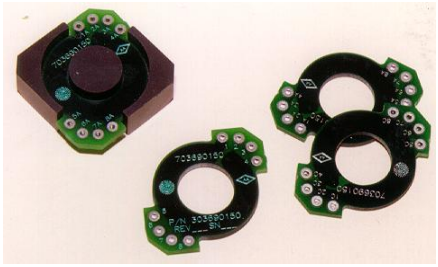


Tramst



Demomag

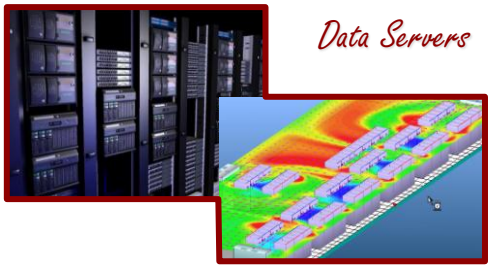




Scope

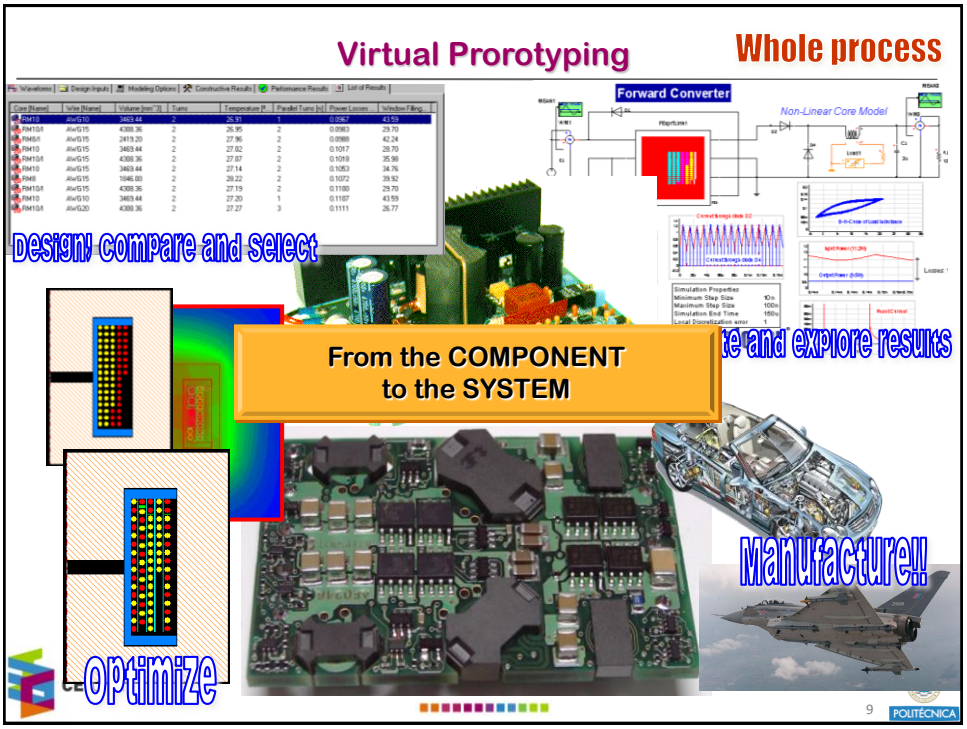
Automovile

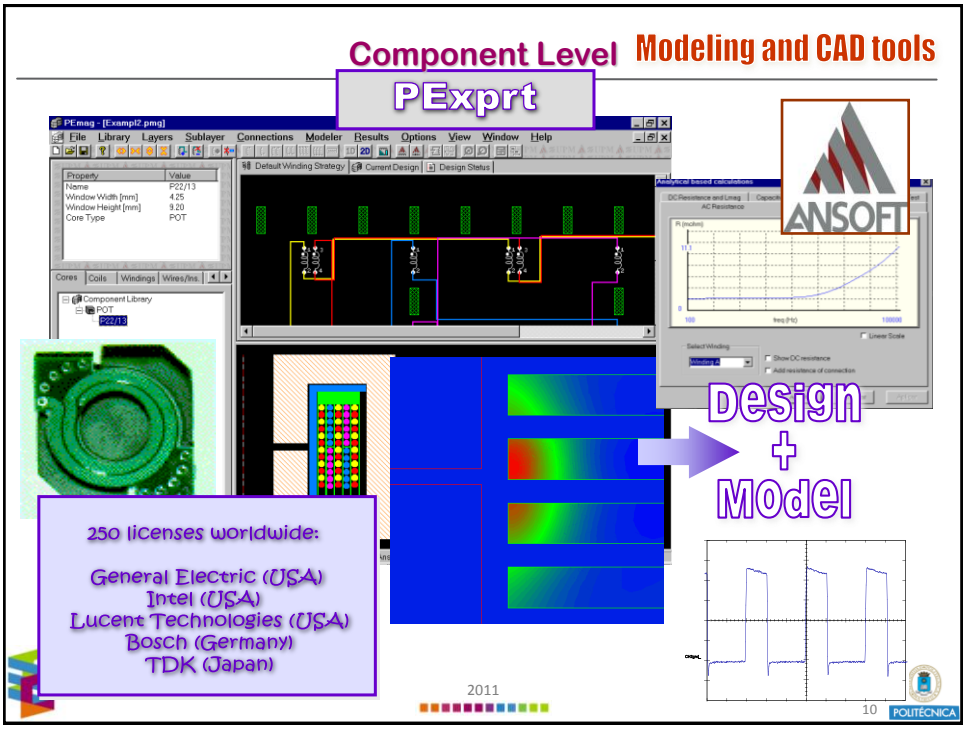
Data Servers

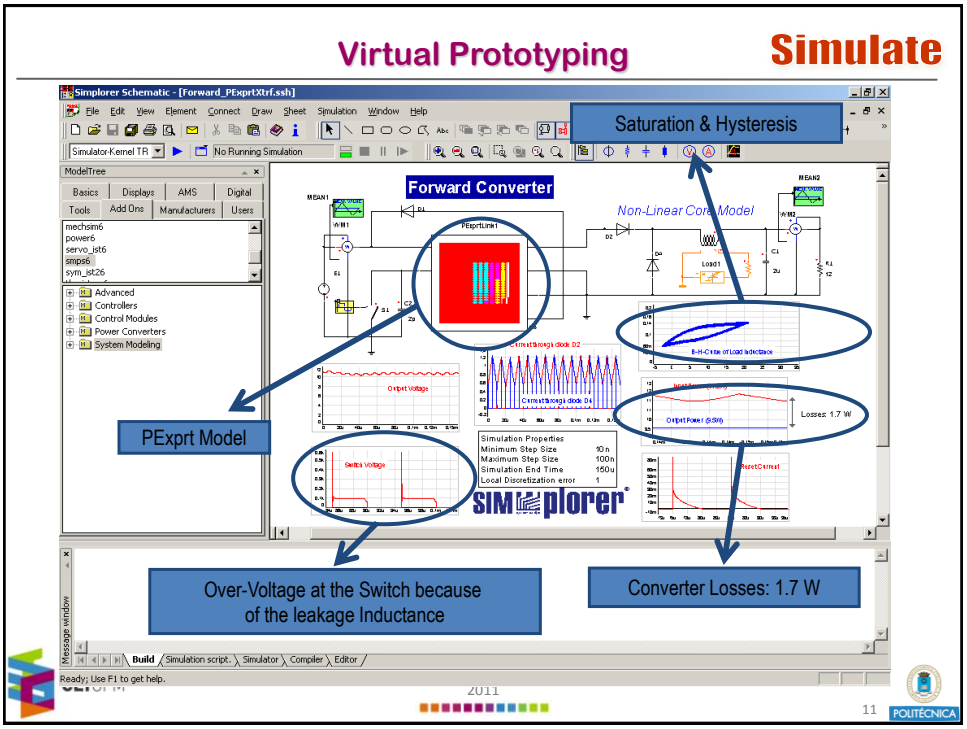


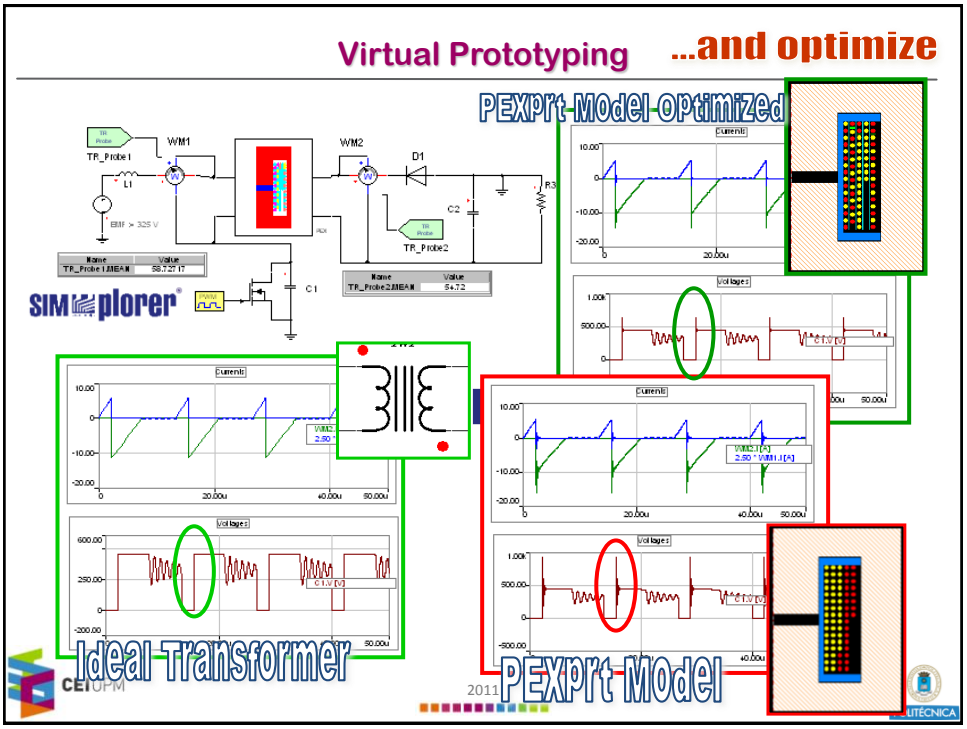
Aeronautics

Aerospace

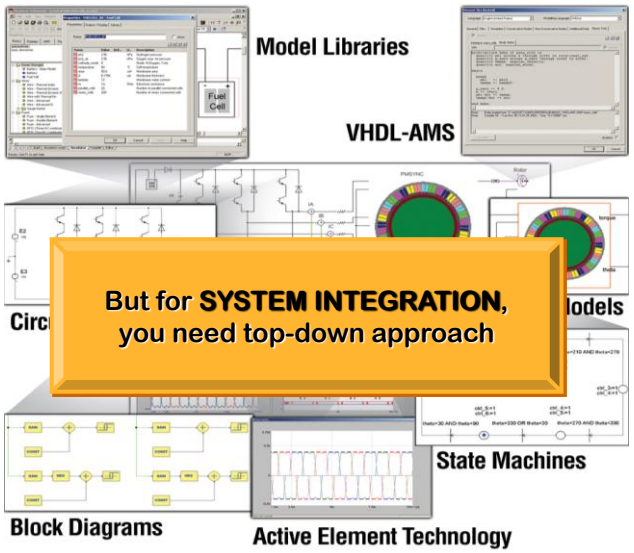

Virtual Prorotyping
Whole process
Forward Converter
Non-Linear Core Model
Design compare and select
From the COMPONENT
to the SYSTEM
te and explore results
Manufacture!!
Optimize
9
POLITÉCNICA


Component Level
Modeling and CAD tools
PExprt
ANSOFT
Design
+
Model
250 licenses worldwide:
General Electric (USA)
Intel (USA)
Lucent Technologies (USA)
Bosch (Germany)
TDK (Japan)
2011
10
POLITÉCNICA


Virtual Prototyping
Simulate
Saturation & Hysteresis
Forward Converter
Non-Linear Core Model
PExprt Model
Over-Voltage at the Switch because of the leakage Inductance
Converter Losses: 1.7 W
SIMplorer

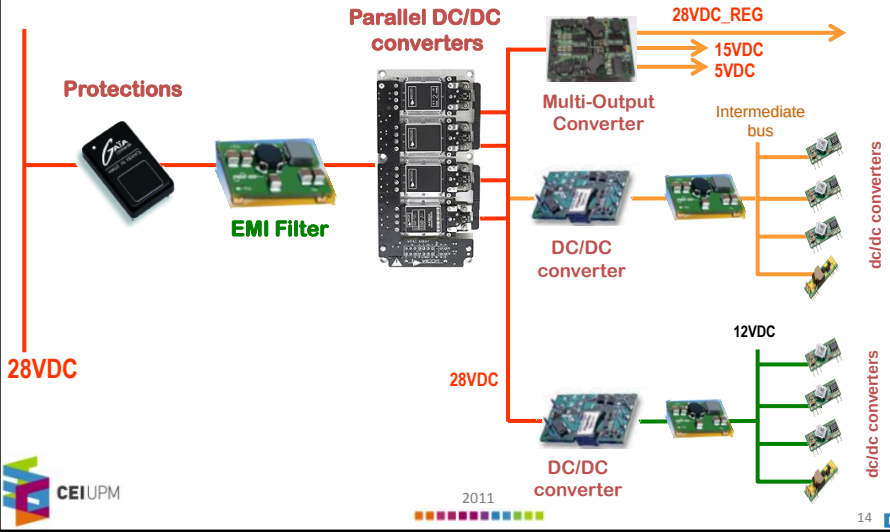

Virtual Prototyping
...and optimize
PEXprt-Model Optimized
SIMplorer
Ideal Transformer
PEXprt Model

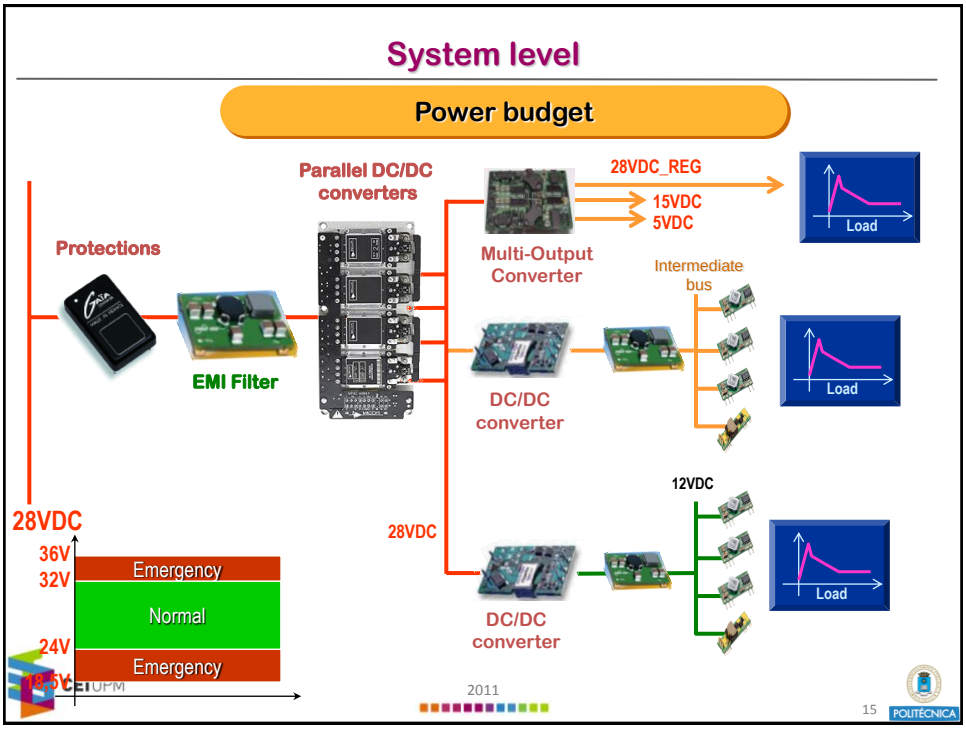
Virtual Prototyping — Whole process

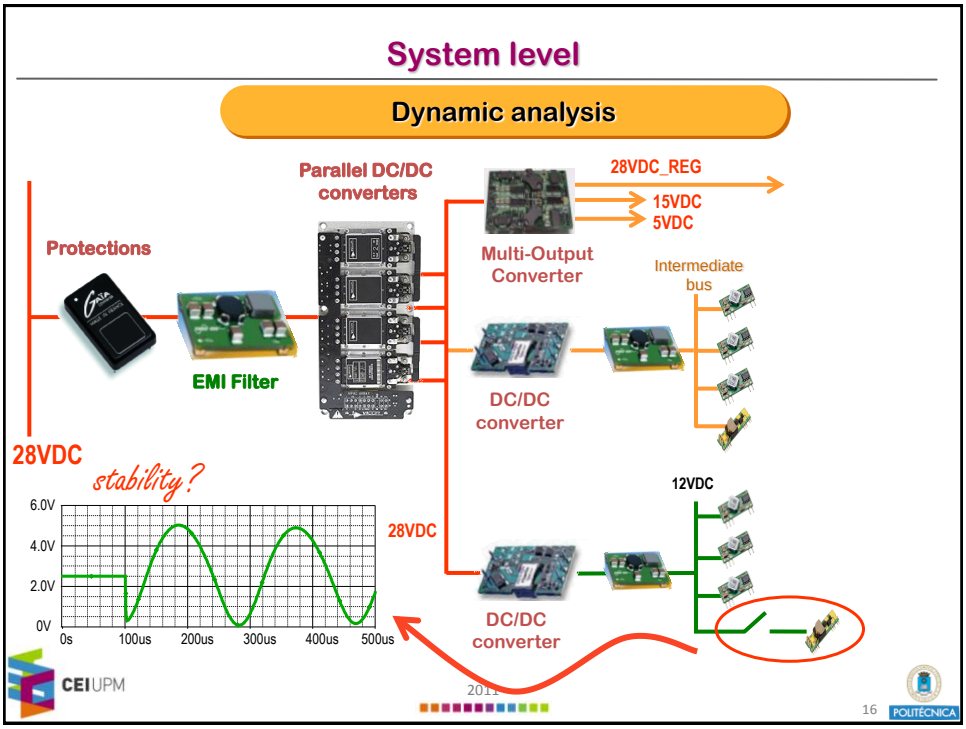


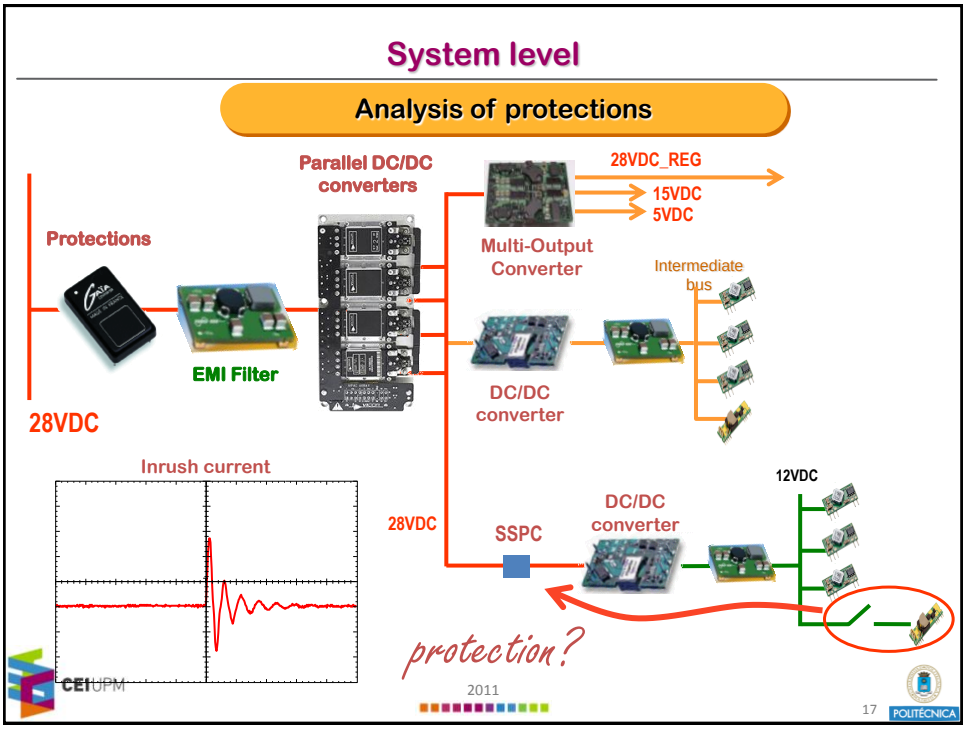
System level

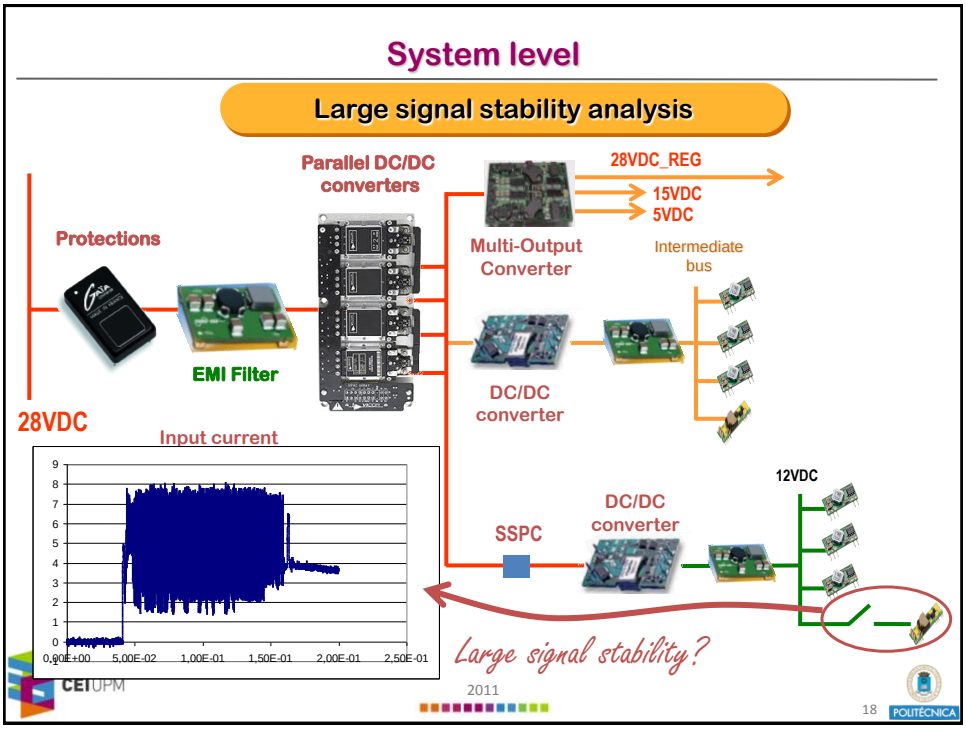
Distributed power system

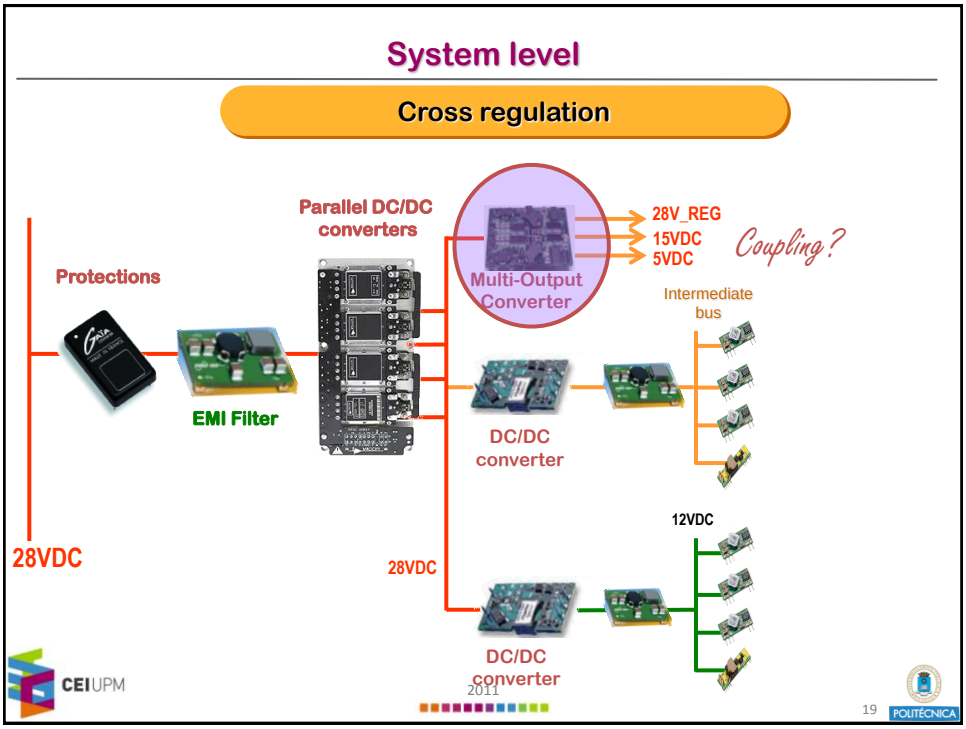


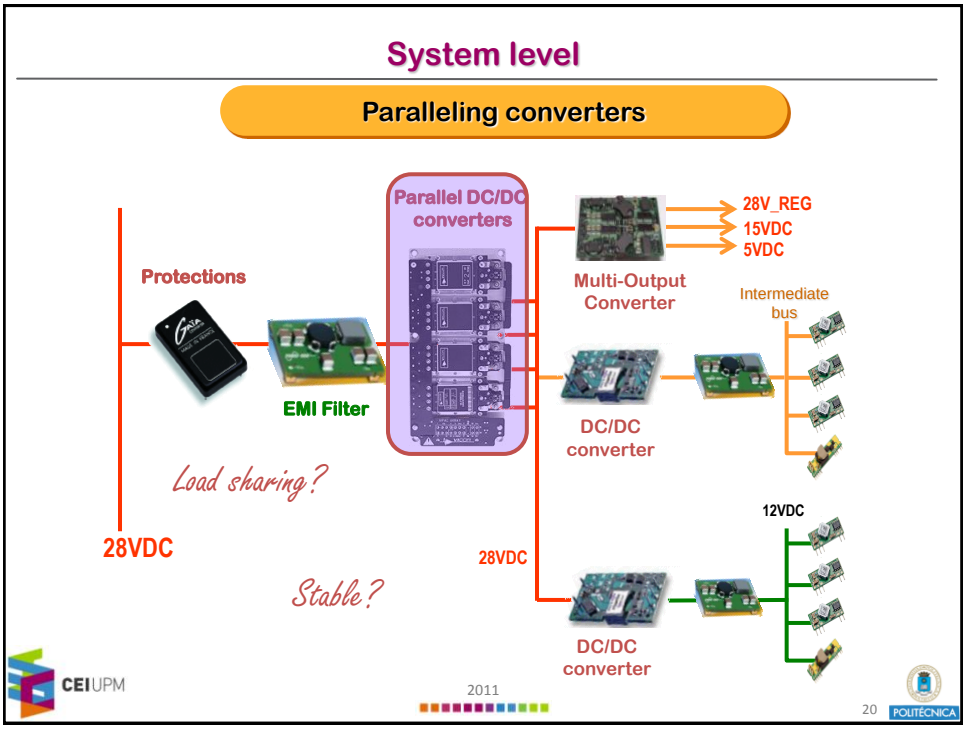

System level
Power budget
Parallel DC/DC converters
28VDC_REG
15VDC
5VDC
Load
Protections
Multi-Output Converter
Intermediate bus
EMI Filter
DC/DC converter
Load
12VDC
28VDC
28VDC
36V
32V
Emergency
Normal
24V
Emergency
DC/DC converter
Load
2011
15
POLITÉCNICA


System level
Dynamic analysis
Parallel DC/DC converters
28VDC_REG
15VDC
5VDC
Protections
Multi-Output Converter
Intermediate bus
EMI Filter
DC/DC converter
28VDC
stability?
12VDC
6.0V
4.0V
2.0V
0V
0s
100us
200us
300us
400us
500us
28VDC
DC/DC converter
CEI UPM
2011
16
POLITÉCNICA


System level
Analysis of protections
Parallel DC/DC converters
28VDC_REG
15VDC
5VDC
Protections
Multi-Output Converter
Intermediate bus
EMI Filter
DC/DC converter
28VDC
Inrush current
12VDC
28VDC
SSPC
DC/DC converter
protection?
CEI UPM
2011
17
POLITÉCNICA

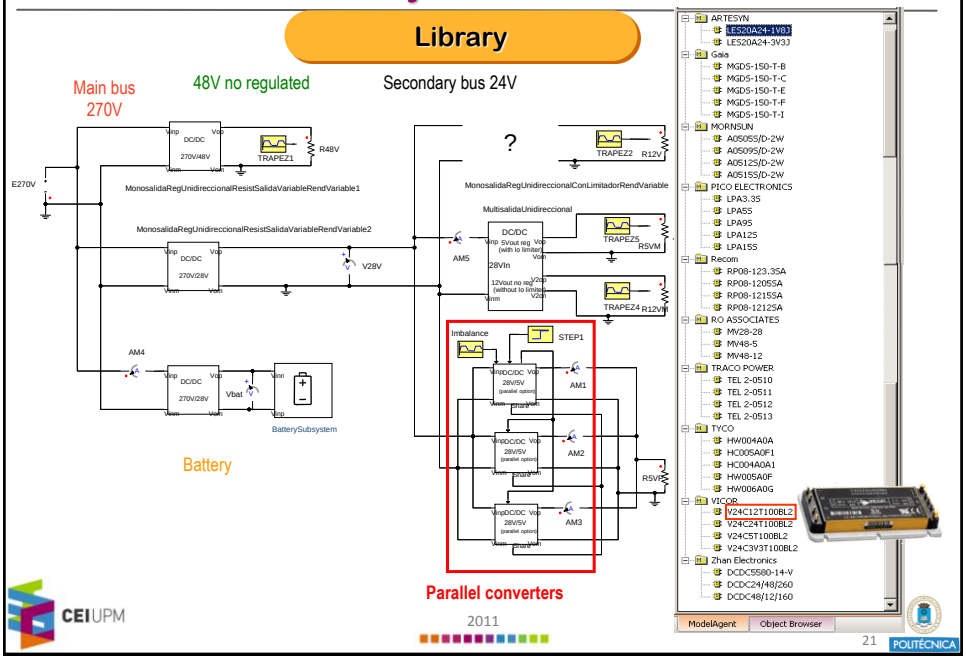

System level
Large signal stability analysis
Parallel DC/DC converters
28VDC_REG
15VDC
5VDC
Protections
Multi-Output Converter
Intermediate bus
EMI Filter
DC/DC converter
28VDC
Input current
12VDC
SSPC
DC/DC converter
Large signal stability?
CEI UPM
2011
18
POLITÉCNICA


System level
Cross regulation
Parallel DC/DC converters
Protections
EMI Filter
Multi-Output Converter
28V_REG
15VDC
5VDC
Coupling?
Intermediate bus
DC/DC converter
12VDC
28VDC
28VDC
DC/DC converter
CEI UPM
2011
19
POLITÉCNICA


System level
Paralleling converters
Parallel DC/DC converters
Protections
EMI Filter
Multi-Output Converter
28V_REG
15VDC
5VDC
Intermediate bus
DC/DC converter
Load sharing?
28VDC
12VDC
28VDC
Stable?
DC/DC converter
CEI UPM
2011
20
POLITÉCNICA

System level

Library

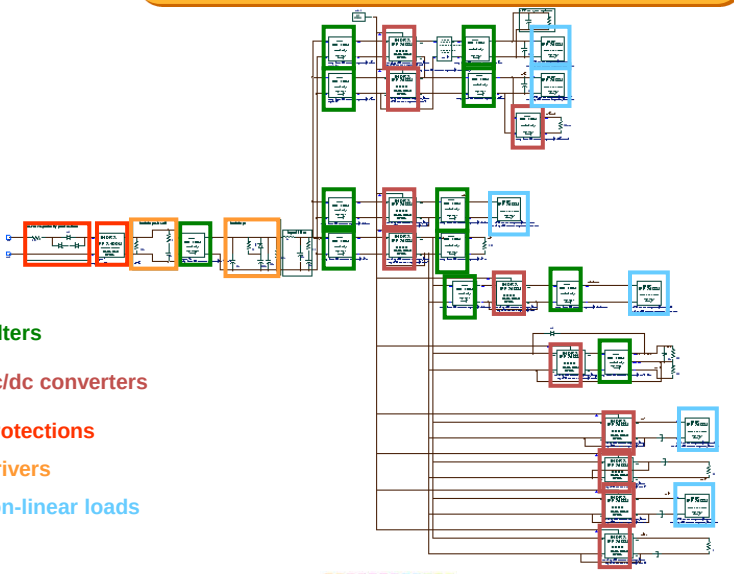


CEIUPM

2011

Validation

SABER® sketch



Filters

dc/dc converters

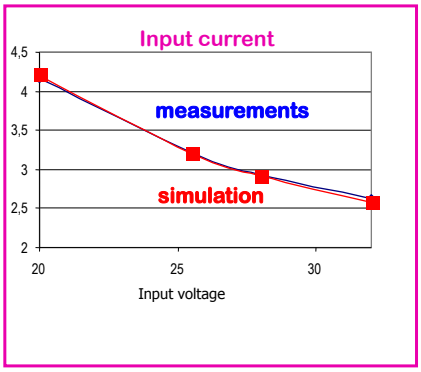
Protections

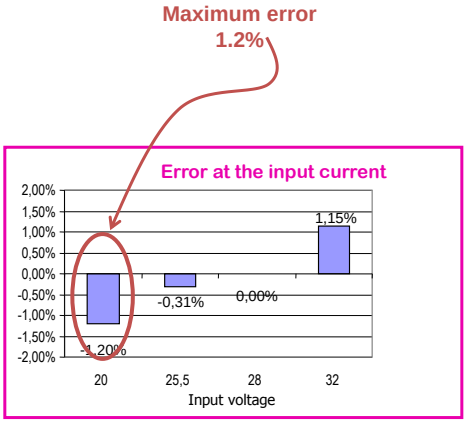
Drivers

Non-linear loads

Validation

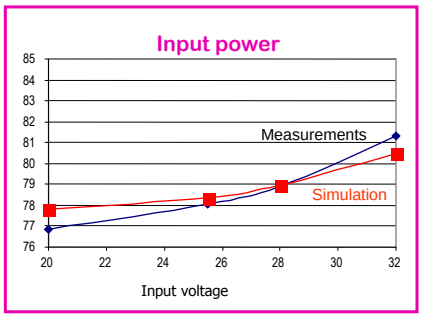
Power Consumptions I

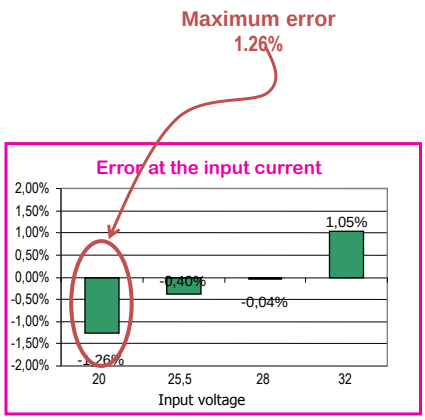




Validation

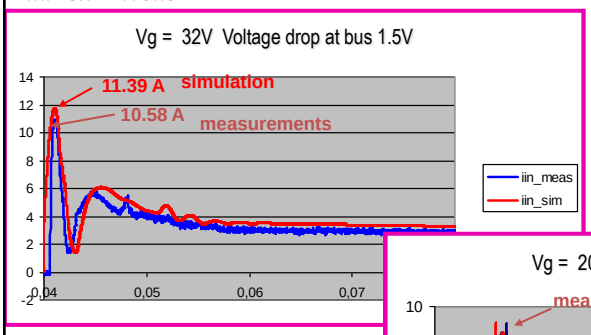
Power Consumptions II

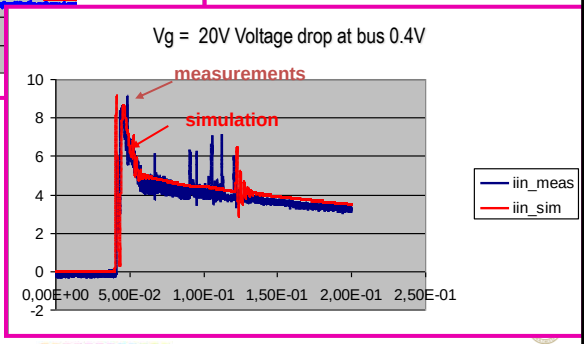




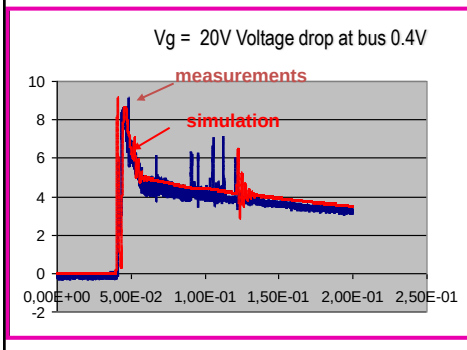
Validation
Transients

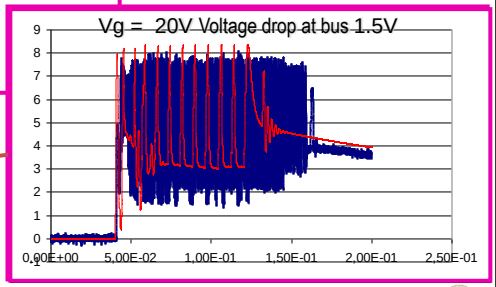
Inrush current





Validation
Start-up





Large signal instability
(during start-up)

Maned Fuel Cell Plane

PHANTOM WORKS BR&TE

Instrumentation panel

throttle
Batt_start_sw
Batt_conn_sw
FC_PLC_cmd

co-simulation

MATLAB SIMULINK

GENERAL_CONTROL

Contactors

HV_BUS

Li-Ion Battery

Inverter

Motor + Load

Fuel-Cell Stacks

FUEL CELLS STACKS

Contactors

SERIES BOOST CONVERTER

Series Boost Converters

Non-linear Loads

SIMplorer

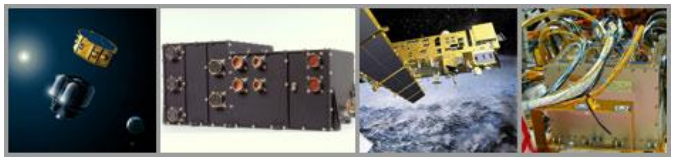
Modeling Power Electronics for Space

EADS ASTRIUM CRISA

Solid State Power Controllers (SSPCs)

Modeling and simulation of solar powered distributed power architectures

LISA Pathfinder



Fuel Cell powered Power Electronics

Comunidad de Madrid

CDTI Centro para el Desarrollo Tecnológico Industrial

EADS DEFENCE & SECURITY

INNOVA "Power distribution and management of High Voltage loads"

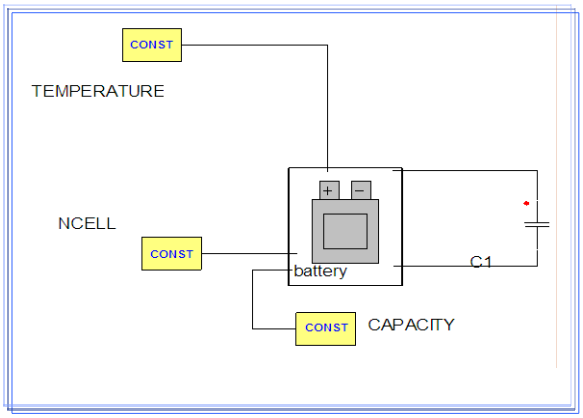
CENIT DEIMOS " Development and Innovation on Polimer Membrane and Solid Oxid Fuel Cells

- More Electric Aircraft Arquitectures modeling and simulation
- High Voltage Distribution Network ($270V_{DC}$)
- Intelligent load management
- Auxiliary Power Units based on Fuel Cells

BATTERY MODELING

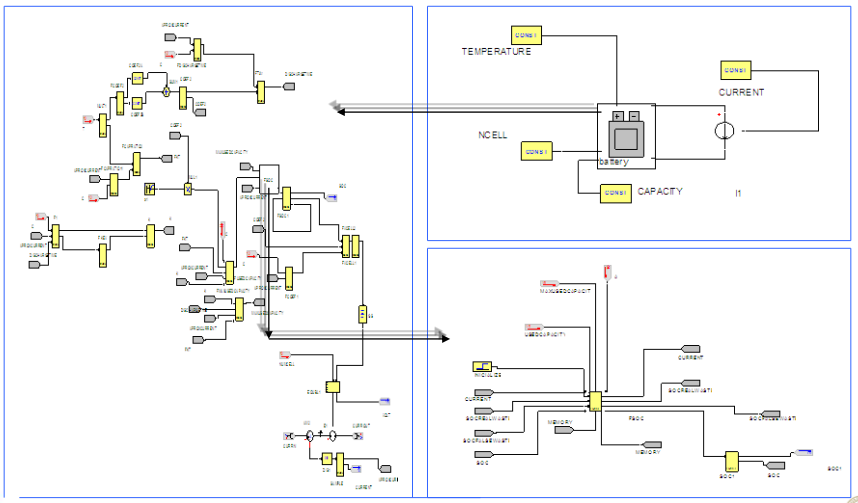
BATTERY MODEL

- INTERNAL PARAMETERS
- INPUTS
  - -INSTANT CURRENT
  - -INSTANT TEMPERATURE
  - -NUMBER OF CELLS
- OUTPUTS
  - -STATE OF CHARGE
  - -CELL VOLTAGE
  - -BATTERY VOLTAGE
  - -INSTANT AND GLOBAL DISCHARGE TIME



Simplorer Development

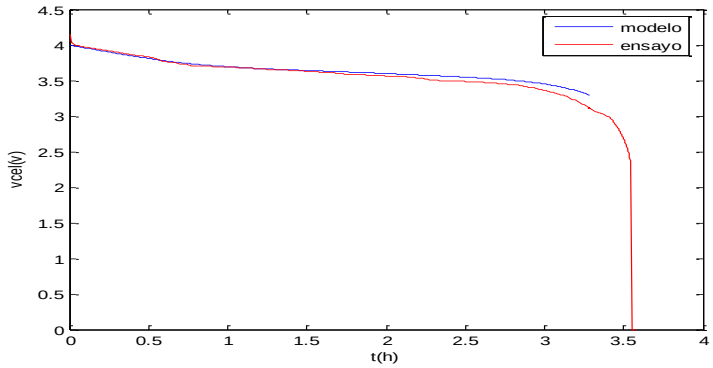
BLOCKS



Validation

- LI-IÓN
  BATTERY HP 1100mAh 3.7v

Current discharge 0.27C



CEI UPM
Centro de Electrónica Industrial

Circuit Breakers

cei@upm.es

Motivation

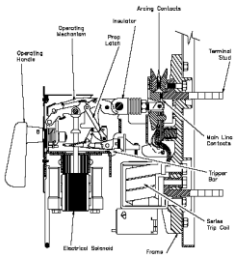
- Every electric circuit requires protection against shortcircuits and overloads.
- The rest of components need to be protected and isolated from the source of failure.
- There are many kinds of switches available:

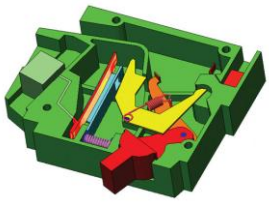
Fuses Circuit Breakers SSPCs

Model scope

Many types of switches - difficult development of a general model if trying to reproduce its physical components.

Air Circuit Breaker





Bimetalic strip

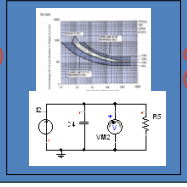
X-ray Thermal Circuit Breaker

Magnetic Circuit Breaker

Behavioral Model

Model I – Calculates the Trip time according to the Tripping-Time Characteristics

Input – I (A)



Output – t (s)

Model II – Data acquisition (Left) and Simimulation Data Comparator (Right)

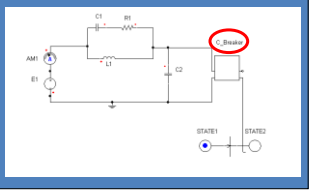
Data acquisition and Look-up Table Configuration

Values can be reset for any device.

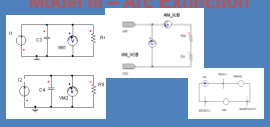
Verification Stage

Verifies Delay Time (MI) vs. Delay Time (Look-up Tables)

Main Circuit

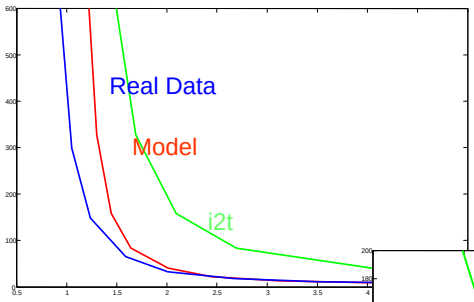


Model III – Arc Extinction



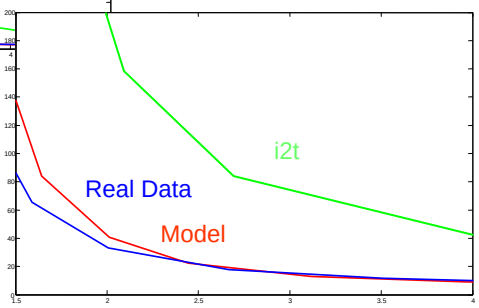
The main strength of this model is that its parameters: R4, R5, C3, C4 can be readjusted to emulate the behavior of any switching device tested.

Results obtained



A true i2t used as a tripping control device predicts a wrong behavior for higher currents.

Correct behavior for the highest currents.



CEI UPM
Centro de Electrónica Industrial

Power Distribution Architectures Design Tool

Leonardo Laguna Ruiz

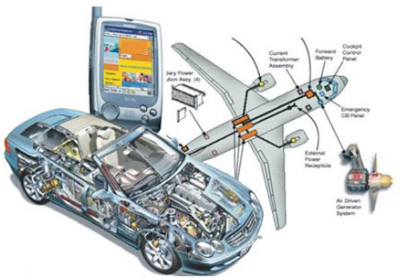
cei@upm.es

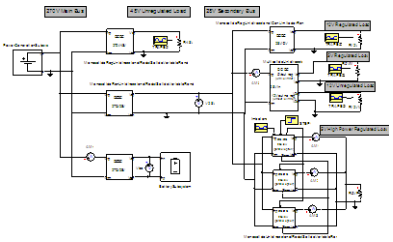
UNIVERSIDAD POLITÉCNICA DE MADRID

POLITÉCNICA

Introduction

- Examples of power systems:
  - Mobile devices
  - Computers
  - Airplanes
  - Automobiles
- Critical design factors:
  - Time to market
  - Size
  - Energy efficiency
  - Cost



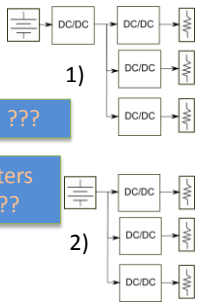


Introduction

- Main problems when designing a power system:
  - Many possible solutions
  - Prototyping is unfeasible

  ✓ Solution: **Simulation**

- Problems with simulation
  - Still many possible solutions
  - Complex models are time consuming



Option 1) or 2) ???

Which converters in each case ???

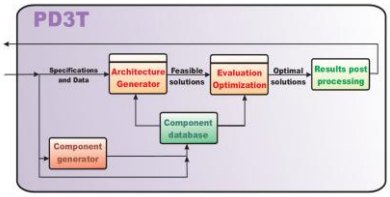
Our approach:
Analyze a LARGE number of solutions with a little less accuracy

After that:
Analyze the BETTER solutions with more detail

Design tool description

- Characteristics of the design tool:
  - Analyze a wide range of possibilities (architectures & components)
  - Establish a trade-off among Efficiency, Cost and Area

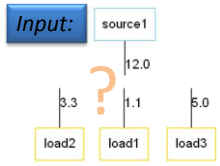
- Other valuable characteristics
  - Follows a Top-Down design methodology
  - Can interact with other tools
  - Provides a generic optimization framework



CEI UPM | Centro de Electrónica Industrial

Example application

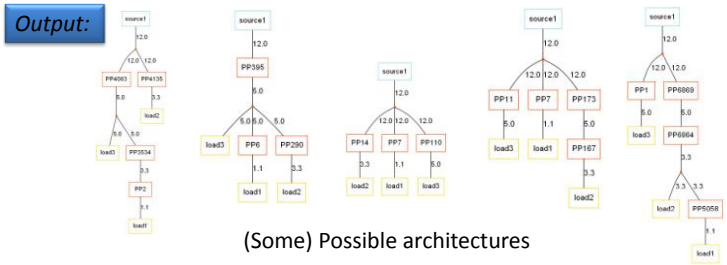
- Feed 3 loads from a source using 100 converters from a database:
  - Source → 12 V
  - Load1 → 1.1 V
  - Load2 → 3.3 V
  - Load3 → 5.0 V



Problem definition

Converter database

Step 1: Architecture Generator



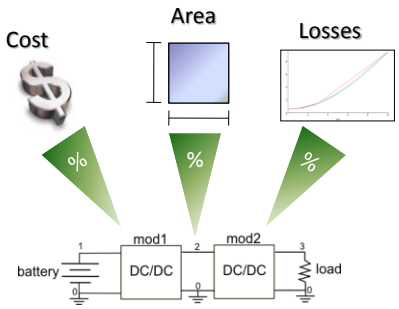
(Some) Possible architectures

Evaluation criteria

Step 2: Architecture and component selection

- Problem specification
  - 16 different architectures: (3-6 converters each)
  - 3 brands, 6 different output power for each converter

Total combinations: 44,113,248
But we want only the best 8



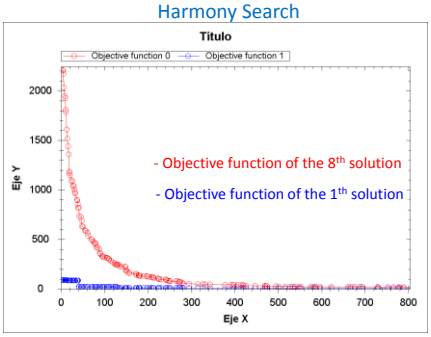
- Selection criteria
  - Cost ≈ cost of components
  - Area ≈ area of components
  - Efficiency: depending on the loads behavior

Optimization (search) of best solutions

- How to find the best 8 among 44,113,248 solutions?
  - Evolutionary algorithms
    - Harmony search
    - Genetic algorithms
    - Tabu search

Using Harmony Search less than 0.05% of solution space is explored to find the optimal solution

Searching the best solutions with Harmony Search



CEI UPM
Centro de Electrónica Industrial

Modeling a Power Delivery Network (PDN)

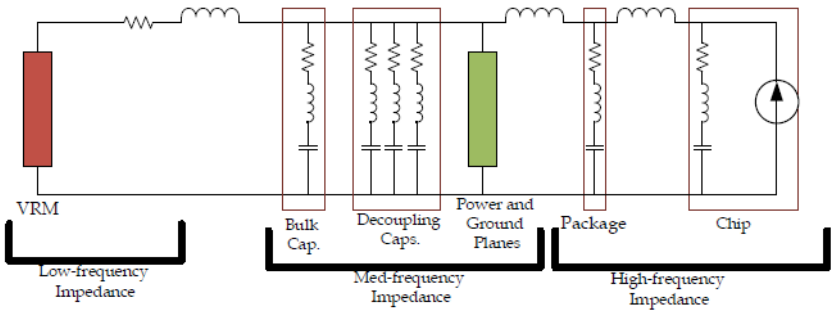
cei@upm.es

Introduction

The power supply cannot be connected directly to the Vdd and Gnd terminals of the IC. It is necessary to use wires, these wires creates both a DC drop and time-varying fluctuation of the voltage. The voltage fluctuation can cause the following problems:

- Reduction in voltage across the power supply terminals of the IC that slows down the transistor or prevents the transistor from switching states.
- Increase in voltage across the power supply terminals of the IC, which creates reliability problems.
- Timing margin errors caused by degraded waveforms at the output of the drivers.

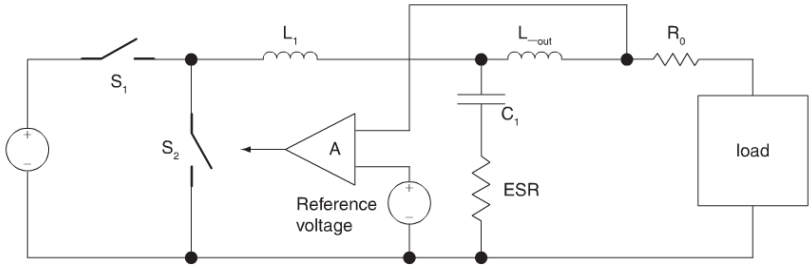
PDN elements and the range of operations frequencies



Nabil, S.M.; El-Rouby, A.B.; Hussin, A.; "A complete solution for the power delivery system (PDS) design for high-speed deigital systems";Design & Technology of Integrated Systems in Nanoscal Era, 2009. DTIS '09. 4th International Conference on; 2009 , Page(s): 179 - 183

VRM

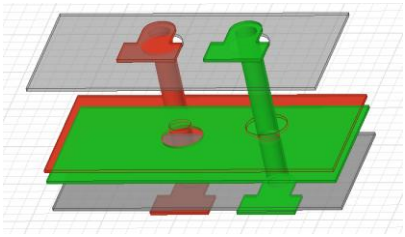
- Provides the power to the chip.
- The main influence is in low frequency (below of megahertz range).

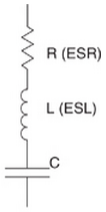


L. D. Smith, R. E. Anderson, D. W. Forehand, T. J. Pelc, and T. Roy, "Power distribution system design methodology and capacitor selection for modern CMOS technology," *IEEE Transactions on Advanced Packaging*, vol. 22, no. 3, pp. 284-291, Aug. 1999.

Decoupling capacitors

- The capacitors are surface mount devices (SMDs) attached to pads on the PCB or package. When SMD capacitors supply charge (or current), the current leaves the voltage plane, travels through the voltage via, flows through the capacitor, and returns through the ground via and then to the ground plane. These contributes to increase the ESL.

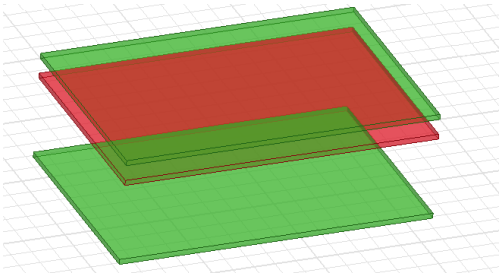




L. D. Smith, R. E. Anderson, D. W. Forehand, T. J. Pelc, and T. Roy, "Power distribution system design methodology and capacitor selection for modern CMOS technology," *IEEE Transactions on Advanced Packaging*, vol. 22, no. 3, pp. 284-291, Aug. 1999

Modeling the planes

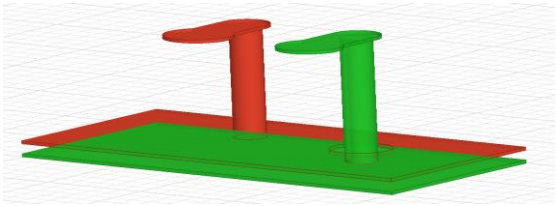
- Planes play a very important role at high frequencies by acting as high-frequency capacitors, serving as conduit for the transportation of current, and supporting the return currents of the signal lines referenced to it. Planes are large metal structures separated by a thin dielectric and are invariably used in all high-frequency packages and boards for power delivery and shielding.



Madhavan Swaminathan; A. Ege Engin, *Power Integrity Modeling and Design for Semiconductors and Systems,* Prentice Hall, 2007.

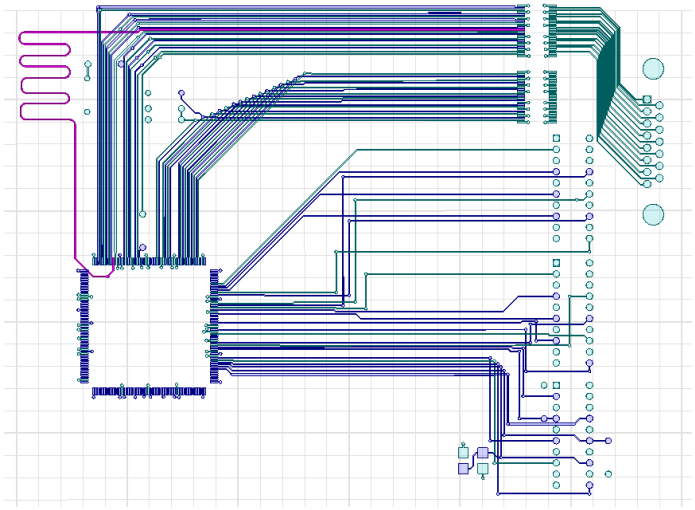
Vias and chip characteristics

- Each new technology generation results in a rapid increase in circuit densities and interconnect resistance, faster device switching speeds, and lower operating voltages. These trends lead to microprocessor designs with increased current densities and transition rates and reduced noise margins. The large currents and interconnect resistance cause large, resistive*IR* voltage drops, while the fast transition rates cause large inductive *LdI*/*dt* voltage drops in on-chip power distribution networks.



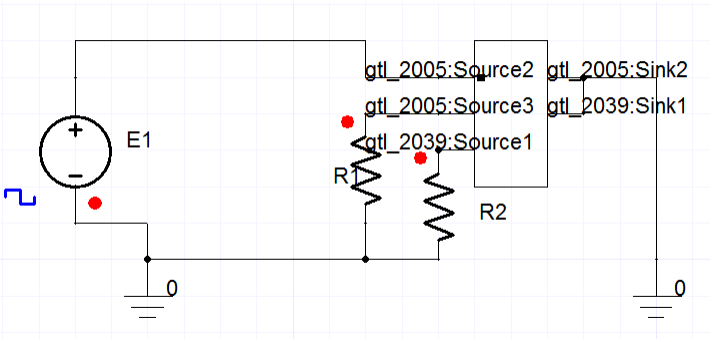
M. Swaminathan, J. Kim, I. Novak, and J. P. Libous, "Power distribution networks for system on package: status and challenges," *IEEE Transactions on Advanced Packaging*, vol. 27, no. 2, pp. 286-300, May 2004

PCB simulated in Q3D Extractor



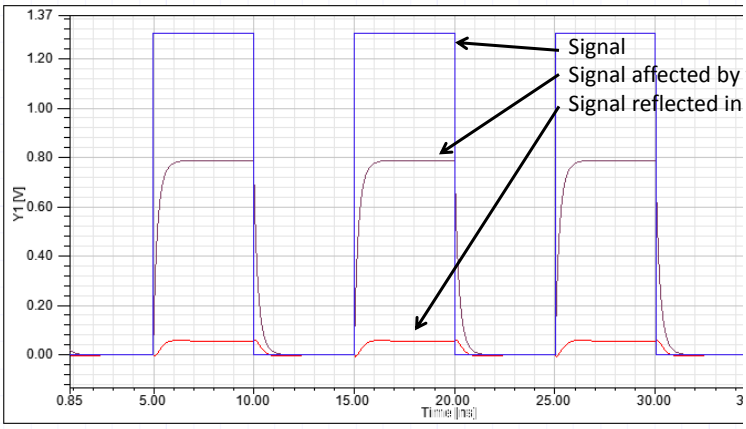
Model in Simplorer

- The parameters extracted form the PCB are simulated using a signal in a trace and showing the efects of this parameters in one point of the trace and in an adjacent trace.



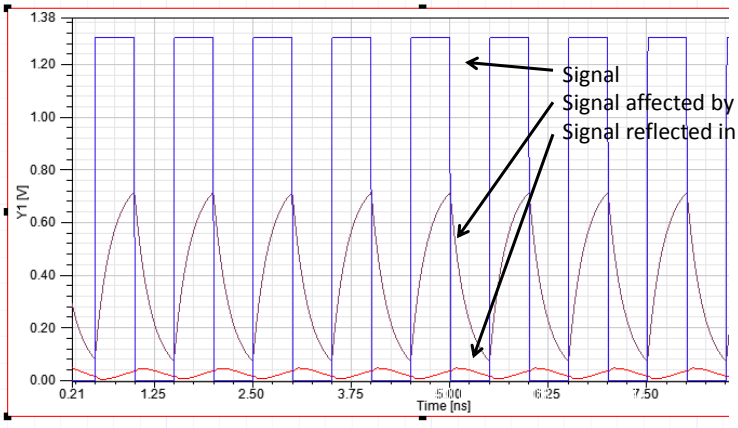
Results @ 100 MHz

- The signal has a small delay and a voltage drop.
- The adjacent trace has a reflected signal.

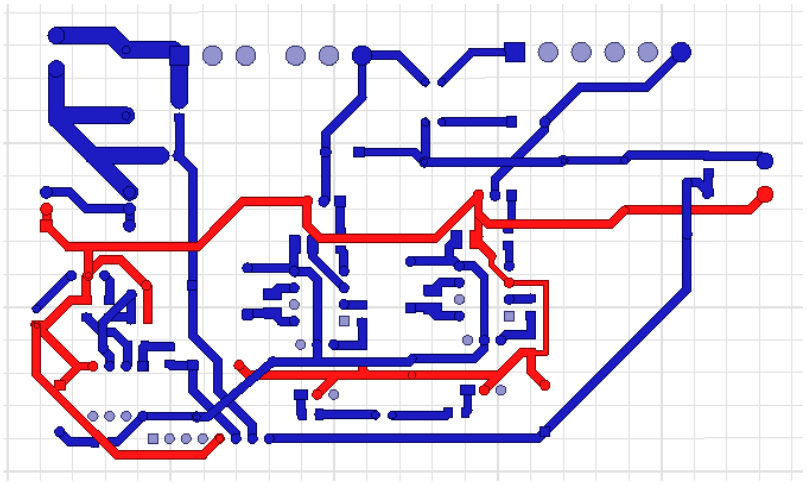


Results @ 1GHz

- The signal is afected by the PCBs parameters.
- The adjacent trace continues having a reflected signal.

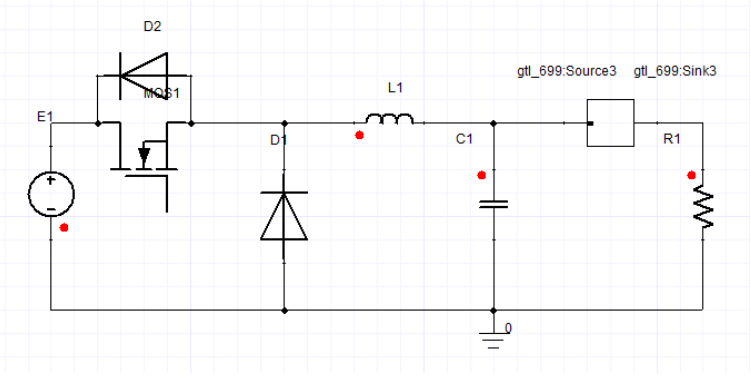


PCB Buck converter simulated in Q3D Extractor



Simplorer simulation

- The PCB of the typical VRM (Buck converter) is simulated with Q3D Extractor and the parameters are simulated in Simplorer.



Results

- The graph shows the output voltage of the VRM before and after the PCB parameters.
- It can be noticed that the voltage after the PCB parameters the voltage is lower.