

Digital Control in Multi-Phase D.C.-D.C. Converters

Angel de Castro, Pablo Zumel¹, Oscar García, Teresa Riesgo, Universidad Politécnica de Madrid (UPM) - División de Ingeniería Electrónica (DIE); 28006 Madrid - SPAIN

Keywords: digital control, custom hardware, field programmable gate arrays, multi-phase converters, interleaving, concurrency control, d.c.-d.c. power conversion.

Abstract

Multi-phase power converters are especially used in applications such as mobile equipments, VRM or automotive power supplies. This is due to their advantages, like increased output current capability, better thermal management, improved dynamic response, reduced EMI and harmonics, and smaller input and output filters. As a consequence, the design space can be re-explored using multi-phase converters.

In this work, digital controllers are proposed for multi-phase converters. They provide advantages that are especially important for these converters and overcome problems difficult to solve with analog controllers. Some of the digital control advantages are capability for managing a large number of driving signals, accurate duty cycle generation, and easy phase-shifting of the driving signals. The proposed controller is based on custom hardware, like Field Programmable Gate Arrays (FPGA), for taking advantage of its concurrent operation in order to generate all the driving signals.

The experimental results show the feasibility of the method, opening interesting possibilities in the control of state of the art power converters.

Introduction

Multi-phase power converters have increased their use in the last years [1]-[5]. Several applications can take special advantage of these converters such as mobile equipments, automotive power supplies or VRM. Some of the advantages that multi-phase converters offer are increased output current capability and better thermal management because of the parallel distribution, and improved dynamic response, reduced EMI and smaller filters because of phase-shifting operation (interleaving). However, its control is a major drawback as several phase-shifted signals are needed.

Given the industrial interest in this technique, several analog controllers have appeared for multi-phase converters. These controllers are usually intended for a small number of phases, usually 2 per controller. However, a higher number of phases could be very interesting for some applications, especially if the available semiconductors integration technologies are used.

Digital controllers can play an important role in this case. Digital solutions are now spreading among power converters control, as they previously did in so many different fields. In fact, digital controllers are used even in power converters in which they mean no qualitative change from analog solutions (only quantitative improvements). In the case of multi-phase power converters, their advantages are much more important as digital control is an enabling technology. For instance, they are the key for increasing the number of phases. With this solution, control complexity for a high number of phases would not be a limiting factor any longer, so power converters would then be optimized according only to power issues and cost. Another main advantage is the possibility to avoid a current loop. Conventional multi-phase converters need a current loop for balancing the current per each phase. Unbalance is caused by components deviation and by duty cycle differences. Digital control eliminates the duty cycle differences almost completely, allowing passive current sharing (no current loop). New control algorithms can also be used thanks to a digital implementation, such as non-linear or adaptive regulators. All these advantages make digital control especially suitable for multi-phase converters.

The rest of the paper is organized as follows. The next section deals with the multi-phase converters characteristics regarding both time and frequency domains. The section after is concerned with current sharing, presenting passive current sharing and its limits. The following section explains the details of multiple driving signals generation, while the fore-last section presents the controller architecture. Finally, some experimental results and conclusions are given.

Multiphase converters

Multiphase interleaved converters consist on paralleling and shifting basic conversion cells, named phases (Fig. 1). The phases can be implemented with any topology (buck, boost, flyback, etc). The main features are:

- paralleling power stages (using more than one converter, but each of them smaller) implies dividing energy conversion among the different converters (space distribution); this yields losses distribution, and therefore a better thermal management if discrete components are used; moreover, a higher current capability is also achieved and the designer has an additional degree of freedom for the design optimization;
- phase-shifted operation provides a distributed energy conversion in time as shown in Fig. 2 (time distribution); this implies that smaller filters are needed, and that a better dynamic response is achieved; moreover, high frequency harmonics can be also dramatically reduced, improving the EMI performance of the converter.

Time domain description

For simplicity, a buck converter is considered. The results can be easily extended to other topologies.

When M converters are connected in parallel and shifted, the output current is the sum of all output currents. Average currents are added, that is the goal of connecting converters in parallel. On the other hand, due to the shifting of the output current ripple of the

¹ Pablo Zumel is currently at the Universidad Carlos III de Madrid, in the Electronic Engineering Department

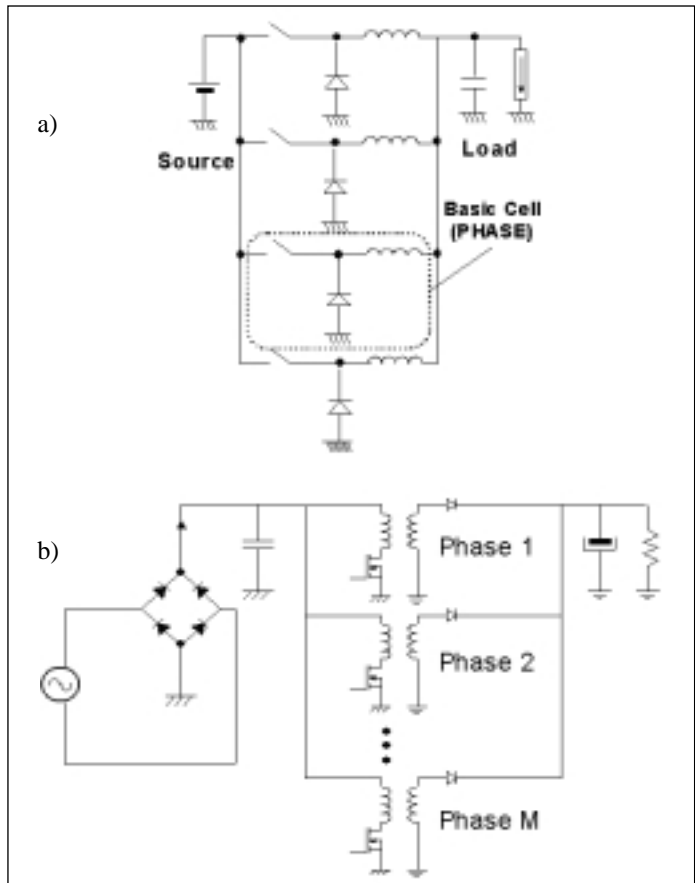


Fig. 1: (a) Interleaved buck converters (b) Interleaved flyback converters for an a.c.-d.c. application

different converters, the total output current ripple is reduced, even fully cancelled for some specific duty cycles. This allows increasing the phase current ripple obtaining the same total output current ripple, and then reducing the equivalent inductance, which is the parallel of all phase inductances. As a result, the dynamic response of the converter is improved.

The output current cancellation factor, or simply cancellation factor, represents the ratio between the inductor current ripple, or phase ripple, and the total output current ripple, which is the sum of all inductor currents (see Fig. 2(a)). This can be calculated considering the number of phases where the inductor current is increasing, and the number of phases where the inductor current is decreasing, for a given duty cycle and number of phases. Assuming continuous conduction mode in a buck converter, the cancellation factor is:

$$F_C = \frac{\Delta I_{OUT}}{\Delta I_{PHASE}} = \frac{d_{eff} \cdot (1 - d_{eff})}{d \cdot (1 - d)} \cdot \frac{1}{M} \quad (1)$$

$$d_{eff} = M \cdot d - \text{int}(M \cdot d) \quad (2)$$

where ΔI_{OUT} is the output current ripple, ΔI_{PHASE} is the phase current ripple, d the actual duty cycle, d_{eff} is the effective duty cycle, M is the number of phases and $\text{int}(x)$ is the integer part of x .

In the case of input current in a buck interleaved converter, the ratio between the ripple in the total input current, and the ripple in the phase input current, is always 1 (Fig. 2(b)). The edges in the input current appear directly at the input terminal, and then there is no ramp cancellation as in the output current. The ratio between the input ripple current and the input average current is inversely proportional to the number of phases:

$$\frac{\Delta I_{IN}}{I_{IN}} = \frac{1}{M} \quad (3)$$

Fig. 3(a) shows the equivalent inductance reduction $L_{eq_multiphase}/L_{single_phase}$ as a function of the duty cycle and the number of phases. This inductance reduction is made keeping the output current ripple constant. Fig. 3(b) shows the cancellation factor vs. the duty cycle. In some points the output current ripple can be zero for any value of phase inductance. It means that if the converter works in these points the inductance can be reduced as much as desired. However, the phase inductance reduction has a drawback: losses increase with the phase ripple. A good lower limit for the phase inductance could be the critical inductance, i.e., the converter is in the boundary between CCM and DCM. In this point the minimum value of the inductor current is zero, and all the energy stored in the inductor is transferred to the output. Negative values of the inductor current are possible, e.g. in synchronous converters (diode has been replaced by a bi-directional switch).

Interleaving allows increasing the output current capability, while the equivalent inductance is reduced, and then the dynamic response is improved.

Frequency domain description

Frequency analysis of interleaving is useful to evaluate the EMI performance. In this case, the quantity under study is the input current, but the conclusions are also true for the output current and other quantities that are the sum of equal and delayed waveforms.

In time domain the output current ripple is highly reduced or even cancelled in some particular points. In frequency domain certain

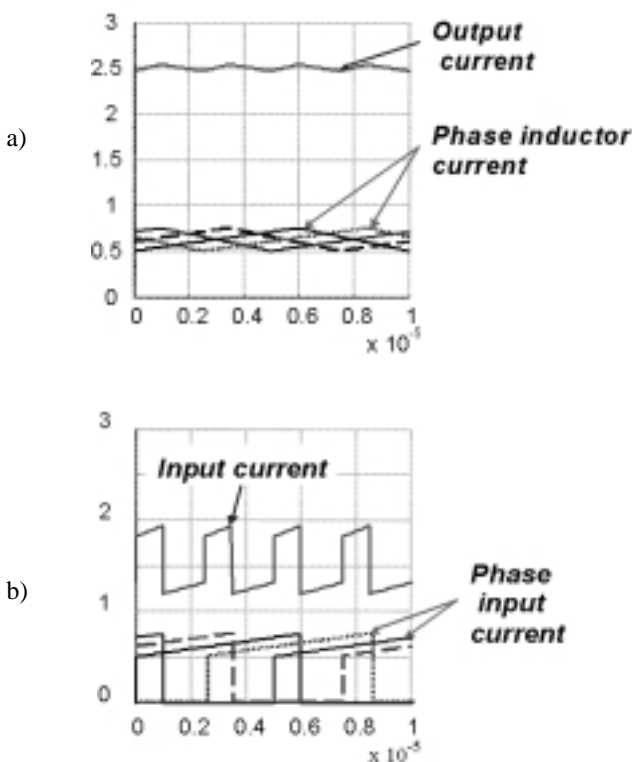


Fig. 2: Input and output current ripple reduction in interleaved converters

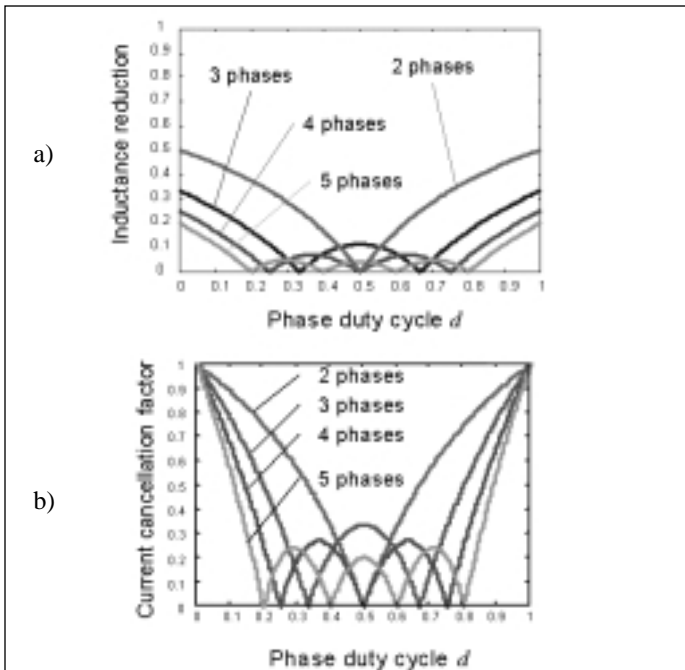


Fig. 3: Effects of interleaving on equivalent inductance for the same output current ripple (a) and output current ripple for the same phase inductance (b)

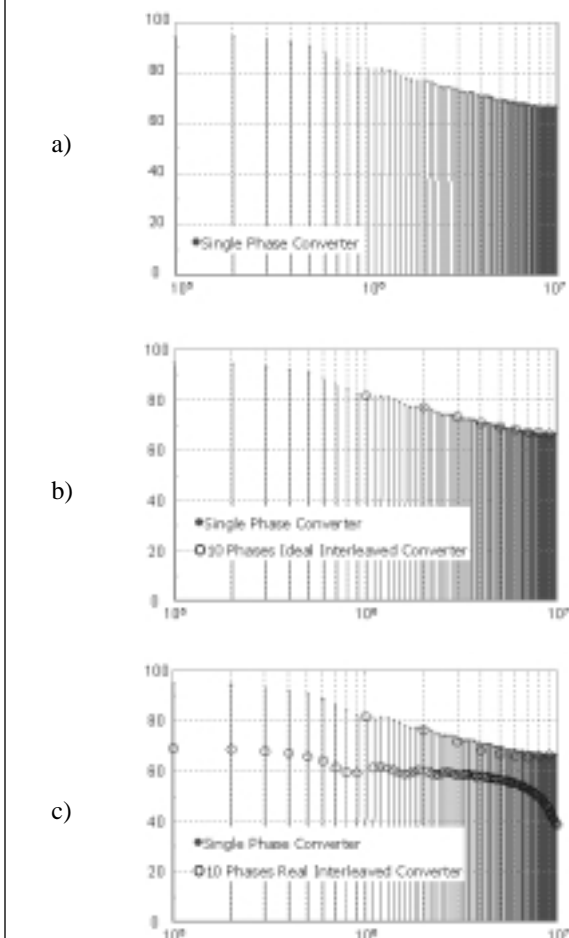


Fig. 4: (a) Harmonics in a single phase converter
(b) Harmonic cancellation in an ideal 10 phase converter
(c) Harmonics attenuation in a real 10 phase converter

harmonics are cancelled for any duty cycle, assuming the ideal case (Fig. 4(a) and Fig. 4(b)). The total input current contains only harmonics whose order is a multiple of the number of phases. In an M phases interleaved converter, the first harmonic to appear is the M th harmonic, the next one the $2M$ th, and so on. The higher the number of phases, the more harmonics cancelled. In the ideal case the expression of harmonic of order n of the input current is:

$$c_n|_{total} = \begin{cases} M \cdot c_n & \text{If } \frac{n}{M} \text{ is a whole number} \\ 0 & \text{If } \frac{n}{M} \text{ is not a whole number} \end{cases} \quad (4)$$

Non idealities of the converter, such as a different duty cycle, non perfect phase shifting and different phase current amplitude, are responsible of the non cancellation of harmonics (Fig. 4(c)). However, the harmonic attenuation obtained in actual converters is good enough.

Therefore, interleaving techniques reduce the differential EMI, specially conducted perturbations. Common mode noise depends mainly on the parasitics, since the energy is not intended to go from the input to the output through the common mode paths. Reduction of the common mode EMI by interleaving is expected to be less important than differential mode EMI reduction.

This property of the interleaved converters is very useful in applications such as PFC [6] or converters very sensitive to EMI, such as CCD power supplies, etc.

Optimal number of phases

One of the most interesting questions for the designer of interleaved converters is: how many phases are the optimal for my application? This is a not very easy question to answer, because there are many factors involved in this issue, such as cost, size, losses and dynamics.

In general, the optimal number of phases depends on the application and on the technology. From the point of view of MOSFET losses, the resistive losses decrease with the number of phases, and capacitive losses increases with the number of phases. There is a local minimum that depends in each case of the product ($R_{DS(on)} \cdot C_{eq}$), where C_{eq} is the equivalent capacitance taking into account the output capacitance and the gate charge. Considering also the inductor design, the optimal number of phases in a given application does not grow indefinitely. For each technology, there is an optimum number of paralleled MOSFET and inductors to minimize the losses.

Input and output filter reduction must also be taken into account. The more the phases, the smaller the filters required. This implies mainly cost and size reduction, while losses are slightly improved. Therefore, EMI filter reduction can also be considered in the choice of the number of phases.

Control complexity can be a limiting factor in interleaved converters, since an analog controller for a many phases converter is very complex. In general, the existing interleaving applications have a relatively low number of phases.

Leaving the controller aside, and taking into account factors such as losses, cost and volume, the optimal number of phases could result quite high (20-40) for some applications. With these designs, losses, cost and size are reduced, besides better dynamics and lower EMI generation. The enabling factor in this case is very often the controller.

Current sharing

There are two main alternatives to equalize the average current in interleaving converters: active current sharing, and passive current sharing.

Active current sharing means that the current in each phase is sensed and adjusted to the corresponding value by a current control loop [7], ensuring an equal current distribution among phases. This system increases complexity and cost when a large number of phases is used. The results in terms of average current equalization are very good.

Passive current sharing operates in open loop with respect to the current. The current is not adjusted to the desired value, but the difference between the actual current and the desired value is kept under acceptable limits by design. A way to achieve passive current sharing is to ensure low tolerances in the component characteristics and the controller to guarantee a good current equalization.

D.c. current distribution depends mainly on two factors [8]: the d.c. resistance of each phase (MOSFETs, layout and inductor), and the effective duty cycle applied to each phase.

The second factor is more critical, since for very small duty cycle mismatch the current mismatch can be quite high (Fig. 5). The effective duty cycle of the voltage applied to the phase inductor depends on the tolerance of MOSFETs and drivers and on the controller characteristics. MOSFETs and drivers can produce different delays on the voltage transitions, and then a different actual duty cycle of the voltage applied to the inductor. The d.c. current mismatch due to duty cycle depends also on the d.c. phase resistance, usually expressed in terms of losses. The lower the d.c. phase resistance, the higher the d.c. current mismatch for the same duty cycle difference.

On the other hand, the controller must be able to provide very small tolerances of the duty cycle. The duty cycle mismatch provided by analog controllers is too high, disabling passive current sharing. Nevertheless, digital controllers can provide a tightly duty cycle dispersion, so passive current sharing is feasible keeping the tolerances of MOSFETs and drivers under reasonable limits.

As an example, considering losses due to d.c. phase resistance of 2 %, the duty cycle mismatch should be at most 0.01 % to achieve a d.c. current mismatch of 10 %. This is only possible if digital controllers are used. In general, digital controllers can guarantee a current mismatch small enough while analog controllers can not.

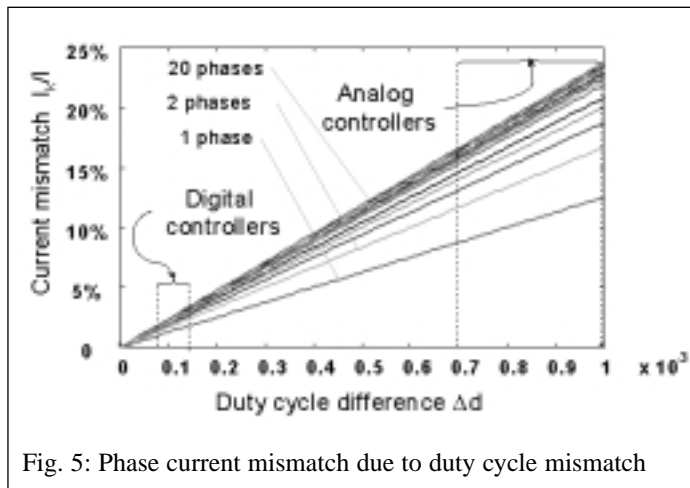


Fig. 5: Phase current mismatch due to duty cycle mismatch

DCM operation is the other way to achieve passive current sharing [9]. Since the inductor current is reset every switching cycle, the average value of the phase currents are very close to each other and the current mismatch is less sensitive to factors as semiconductors or controller characteristics.

Multiple driving signals

Interleaved converters seem to be a good option to consider in a wide range of applications. However, the controller is the most limiting factor, as we have seen. Digital controllers can solve this problem.

Analog commercial controllers are available for a low number of phases (2-12). If a higher number of phases is required (20-40), more chips are needed. It means that analog controls for a high number of phases are very complex in terms of components count. Other researches have been done in this field [10]. Modular approaches with a common bus to adjust automatically the shifting between converters have been proposed, and they are very interesting for systems with many converters, but more difficult to apply in a single interleaved converter.

Controlling multi-phase converters implies generating multiple driving signals, as each phase needs its own gate signals. Consequently, the number of signals to be generated is proportional to the number of phases. A work-around for this problem would be to use the same driving signals for all the phases, but in this way, the interleaving advantages would be lost (such as reduced ripple and input/output filters). In the other extreme, another possible solution would be to control each phase independently. This would lead to a waste of resources and to a complicated current balance, as any minimum difference in the controllers would unbalance the currents drastically.

To solve this problem, a unique control signal is generated, but it is phase-shifted for the rest of the phases. There is only one controller (i.e. only one duty cycle is generated for PWM converters) which produces the driving signal that is phase-shifted.

The phase-shifting operation is in fact a delay equal to the switching period (T_{switch}) divided by the number of phases (N_{phases}):

$$delay = \frac{T_{switch}}{N_{phases}} \tag{9}$$

Each phase is delayed from the previous one for this time (9), so the driving signals are distributed uniformly along the switching period. The result is reflected in Fig. 6.

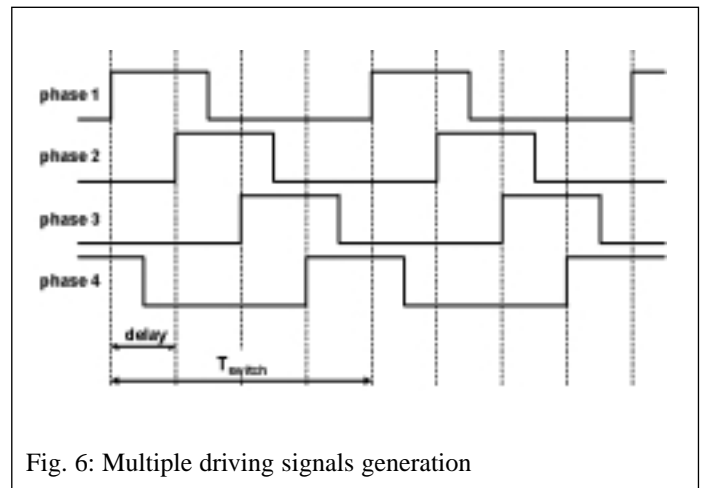


Fig. 6: Multiple driving signals generation

Implementing the phase-shifter by analog means leads to a complicated solution whose complexity grows with the number of phases. Once the phase-shifter is constructed, any change in the number of phases or switching frequency implies physical changes. A digital solution [11] is much more flexible and does not grow proportionally to the number of phases, as a single-chip solution is always possible (even for a large number of phases).

Among digital controllers, those based on microprocessors or DSPs are the most popular. Many DSPs include a block which can be configured as a PWM generator. This is valid for one-phase converters, as only one driving signal is generated. An external block must be added for multi-phase converters, because generating all the driving signals via software would cause a huge amount of interrupts, degrading the controller performance.

The sequential nature of the microprocessors and DSPs, which execute one instruction after the other, is a drawback for controlling many signals simultaneously. Therefore, the phase-shifter is usually implemented using concurrent devices, such as FPGAs or PLDs. All the logic in these devices is executed continuously and concurrently, which makes them especially suitable for generating multiple driving signals. In fact, some DSP-based controllers include an FPGA or PLD² for this task [12]-[15]. In these cases, the DSP is in charge of the control law and the FPGA generates the driving signals. This hardware scheme is reflected in Fig. 7.

However, once an FPGA is included it is more reasonable to use it for all the control tasks. The solution that we propose is substituting the DSP by an FPGA which is in charge of both the control law and the driving signals generation. This solution has been successfully used in previous cases [16]-[18], showing the feasibility of the method. Following this solution, the hardware scheme becomes the one shown in Fig. 8. The following section explains in detail the internal architecture of the proposed controller which has been integrated in an FPGA.

The FPGA can be substituted by an ASIC (Application Specific Integrated Circuit) reducing size and control losses. This would be an equivalent solution with the same advantages, as it also uses concurrent operation. As we see, using concurrent logic devices, new applications are possible for digital controllers. Multi-phase converters are a good example. Low-power applications can also benefit from digital controllers integrating the controller and the converter altogether. Anyhow, the digital controllers' field can be re-explored when concurrent devices are taken into account.

Control architecture

The controller is divided into several blocks in order to make the design process easier. Each block is in charge of a specific task, so it can be developed independently of the other parts. This feature allows easy reconfiguration and reutilization of the different blocks for other designs.

The main two blocks are in charge of the control law and the driving signals generation respectively (see Fig. 9). The block that implements the control law (Duty Controller) receives the output voltage (V_{out}) through the A/D converter. Its purpose is to keep V_{out} in the target value, as this is the controller of a d.c./d.c. converter. In order to do so, it calculates the duty cycle that is imposed on the switches. The duty cycle is then sent to the second main block (Signal Generator) that converts the duty cycle to on/off signals like those shown in Fig. 6. There is no current loop as we

² FPGAs (Field Programmable Gate Arrays) and PLDs (Programmable Logic Devices) are very similar in their behaviour and differ only in the technology they use. We will use the term FPGA for referring to both of them.

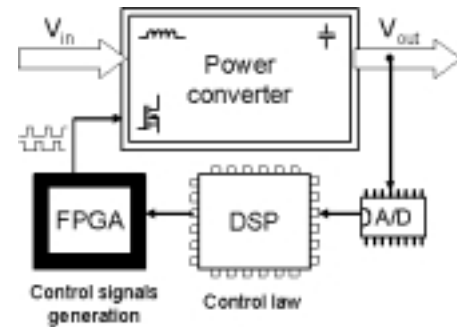


Fig. 7: Hardware scheme with DSP & FPGA

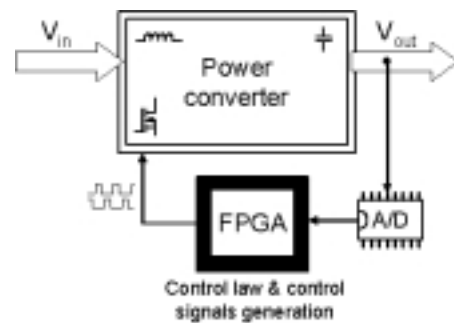


Fig. 8: Hardware scheme with FPGA

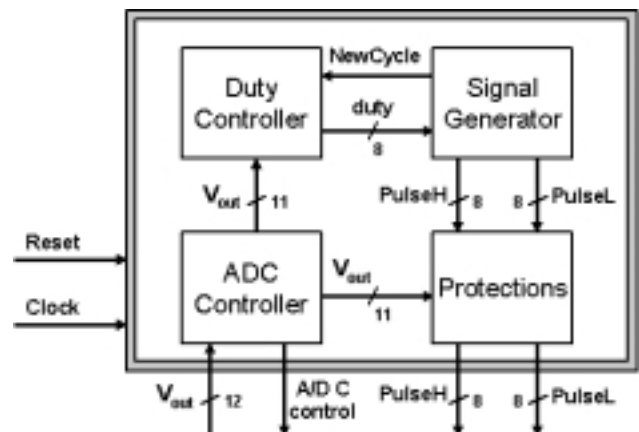


Fig. 9: Controller internal architecture

are using passive current sharing trusting in the digital capability to guarantee minor duty cycle dispersion.

Apart from the main two blocks, there are two other blocks in the controller. One of them is in charge of controlling the A/D converter (ADC Controller). It sends the necessary signals for the correct operation of the conversion and it also translates the incoming data to the internal format used by the rest of the blocks (in our case, the A/D converter sends a 12-bit signed integer, but we use an 11-bit unsigned format filtering atypical data due to noise).

The last block is devoted to protections. Thanks to the FPGA concurrency, there is no drawback in performance when adding new protections. All the logic is executed concurrently, so the protections do not interfere with the rest of the blocks. Another important advantage is that no new hardware is necessary for adding these protections, as the FPGA is also in charge of them. All the

Phase-1	Phase-2	Phase-3	Phase-4	Phase-5	Phase-6	Phase-7	Phase-8
4.21A	4.20A	4.35A	4.40A	4.29A	4.28A	4.46A	4.60A

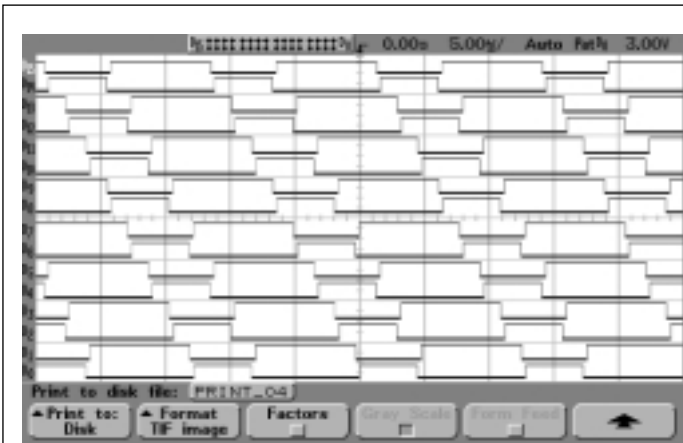


Fig. 10: Driving signals generated by the FPGA for each phase (experimental)

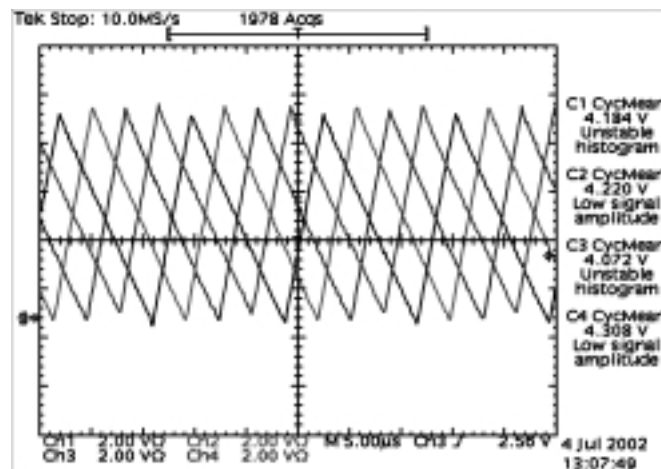


Fig. 11: Currents in phases 1, 3, 5 and 7 (experimental)

desired protections can be added with the only requirement of limiting their resources to the empty area in the FPGA. We have implemented two protections, but many others are possible:

- V_{out} limitation. Whenever V_{out} exceeds a configurable limit, all the phases turn off.
- Maximum duty cycle. The duty cycle is limited to 0.95 in order to avoid changes in the switching frequency and inductors saturation.

The “Duty Controller” could be implemented using a DSP or even an analog controller, as commented in the previous section. The FPGA would be restricted to the driving signals generation and possibly the A/D converter control. However, FPGAs have proven to be able to implement even complex control laws, allowing a higher integration of the controller. This is the proposed solution, which integrates all the blocks of the controller in a single device. Moreover, the FPGA concurrency allows for a faster execution, opening the way to higher switching frequencies.

Experimental results

In order to validate all the theories proposed along the paper, a multi-phase d.c.-d.c. power converter has been built as a prototype. It is an 8-phase bi-directional buck converter designed for 42 V at the input, 14 V at the output and 400 W as nominal power. Therefore, 16 driving signals are necessary. The digital controller has been designed using a hardware description language (VHDL) and implemented in a Virtex V200E FPGA, from Xilinx™. The FPGA works with a 20 MHz digital clock. The digital-PWM block is based on an 8-bit counter, which allows 256 different duty cycle solutions. The switching frequency when employing this technique is equal to the clock frequency divided by the number of duty cycle solutions, 78.125 kHz in this case.

Thanks to the accuracy of the driving signals generation obtained using an FPGA, no current-loop has been necessary for assuring an acceptable current balance. The on-time sent to each phase differs less than 1ns from each other. Therefore, the duty cycle differs less than 0.01 % from phase to phase. Fig. 10 shows the experimental driving signals generated by the FPGA. As it can be seen, there are two driving signals almost complementary for each

phase, as there are two switches in each phase (bi-directional buck converter). Dead-times (when both switches are off) are programmable thanks to the digital controller, showing other of the FPGA advantages.

Table 1 shows the current per phase under nominal conditions. There are some differences as no current-loop is used, but anyway these differences remain under 10 %. They are due to the series resistance mainly, which can be caused by the inductor, switches and layout. In fact, phase-8 is the nearest phase to the output in this prototype and phase-1 the furthest. Therefore, the layout resistance is supposed to be an important reason for these differences.

Fig. 11 shows the experimental currents in 4 of the 8 phases, also in almost nominal conditions. Phase-shifting is shown clearly in this figure.

Conclusions

Some conclusions can be extracted from the presented work:

- multi-phase interleaved power converters have advantages deriving from parallelism (higher output current capability and better thermal management) and phase-shifting (increased dynamic response and reduced ripple and EMI);
- multiple driving signals need to be generated, which have to be phase-shifted and with an almost equal duty cycle; digital controllers are a suitable solution for these problems, especially those implemented using custom hardware such as FPGAs or ASICs;
- current balancing is a major concern; digital controllers allow passive current sharing, as shown in the experimental results. In this way, the current loop is avoided, simplifying the control architecture.
- digital controllers allow a high number of phases, increasing the design space considerably and opening the possibility of a new generation of multi-phase converters.

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The Authors



Angel de Castro was born in Madrid, Spain, in 1975. He received the M.Sc. degree in Electrical Engineering from the Universidad Politecnica de Madrid, Spain, in 1999, where he is currently pursuing the Ph.D. degree. His research interests include digital control of switching mode power supplies, digital circuits design and smart transducers.



Pablo Zumel was born in Burgos, Spain, in 1973. He received the B.Sc. degree in Electrical Engineering from the Universidad de Burgos, Spain, in 1995, and the M.Sc. degree in Electrical Engineering from both the Universidad Politecnica de Madrid and the Ecole Centrale Paris, in 1999. He is currently pursuing the Ph.D. degree at the Universidad Politecnica de Madrid and works at the Universidad Carlos III de Madrid as Assistant Professor. His research interests include interleaved converters, digital control for power converters and integrated magnetics.



Oscar Garca was born in Madrid, Spain, in 1968. He received the M.Sc. and the Ph.D. degree in Electrical Engineering from the Universidad Politecnica de Madrid (Spain), in 1992 and 1999 respectively. He is an Associate Professor at Universidad Politecnica de Madrid. His research interests are switching mode power supplies, power factor correction, power architectures, and digital control applied to power electronics.



Teresa Riesgo was born in Madrid, Spain, in 1965. She received the M.Sc. and Ph.D. degrees in Electrical Engineering in 1989 and 1996, respectively, from the Universidad Politecnica de Madrid in Spain. Since 1990 she has been working at the Electronic Engineering Division at the same University as Assistant Professor, from 1998 as Associate Professor and from 2003 as Professor. Her main research interests are ASIC design, VLSI test techniques and embedded systems.

Angel de Castro, Pablo Zumel, Oscar Garca, Teresa Riesgo, Universidad Politecnica de Madrid (UPM) - Division de Ingeniera Electronica (DIE); Jose Gutierrez Abascal 2, 28006 Madrid - SPAIN. Tel. +34 91 3363191 - Fax. +34 91 5645966
E-mail: acastro@upmdie.upm.es